Multi-level Inverter Capable of Power Factor Control with DC Link Switches

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Abstract

This Project Proposes a New Multi-Level Inverter Topology Based On A H-Bridge Structure With Four Switches Connected To The Dc-Link. Based On A POD (Phase Opposition Disposition) Modulation Method, A New PWM Method Which Requires Only One Carrier Signal we used. The Switching Sequence is based on Balance on the Capacitor Voltage Is Also Considered. In that Proposed Topology Requires Minimum Number Of Component Count To Increase The Number Of Voltage Level.

Keywords: Multi Level Inverter, Power Quality, Power Factor, DC Link, Switches

Introduction

Due to the increasing demand on the renewable energy sources, grid connected inverter systems are becoming more and more important than ever before [1,2]. For grid - connected operation, the inverter should meet the following requirements.

1. The inverter has to generate a pure sinusoidal output voltage.
2. The inverter output current should have low total harmonic distortion (THD).

Traditionally, two-level PWM inverter is used for grid-tied operation. In case of a two-level inverter, the switching frequency should be high or the inductance of the output filter inductor need to be big enough to satisfy the required THD. To cope with the problems associated with the two-level inverter, multi-level inverters (MLIs) are introduced for grid connected inverter. Several MLI topologies have been suggested so far and they can be mainly classified as three types in Fig. 1; neutral point clamped (NPC), flying capacitor (FC), and cascaded type [3-5]. Advantage of the MLIs is that their switching frequency and device voltage rating can be much lower than those of a traditional two-level inverter for the same output voltage.

Therefore, IGBT switching loss can be reduced significantly and thus the inverter system efficiency can be increased [6-8]. In this paper, a circuit based on a H-bridge topology with four switches connected to the dc-link is proposed as a MLI topology. Fig. 2 shows the proposed MLI. Also it is simple because the proposed PWM method uses one carrier signal for generating PWM signals. In addition, the switching sequence considering the voltage balance

of dc-link was proposed. Finally, the proposed topology of the multi-level inverter is verified by showing the feasibility through the simulation and the experiment.

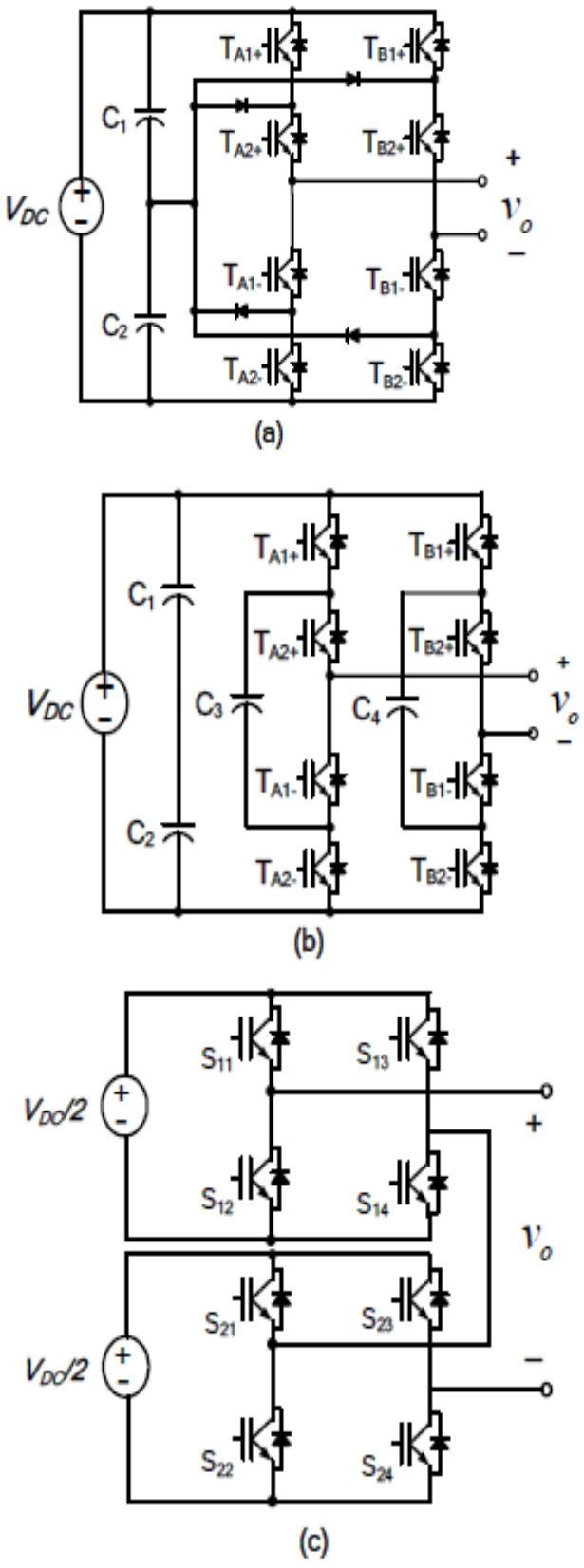

Fig. 1. Topologies of multi-level inverters. (a) Neutral point clamped (NPC) type. (b) Flying capacitor (FC) type. (c) Cascade type.

Proposed Multi-Level Inverter

A. Topology of multi-level inverter

As shown in Fig. 2, the proposed MLI is composed of two dc-link capacitors (C1, C2) and four switching devices (TA +, TA-, TB +, TB -) comprising a H-bridge, and four active switches (TP +, TP -, TN +, TN -) located between dc-link and H-bridge. The voltage across the switching devices in the dc-link (TP +, TP -, TN +, TN -) is VDC/2 and operated at a switching frequency. Whereas, voltage across the switching devices in the H-bridge (TA +, TA -, TB +, TB -) is VDC and the switches (TA +, TA -, TB +, TB -) are switched at a frequency of the fundamental component of the output voltage (e.g. 50 or 60 Hz). Thus, the dc-link switches (TP +, TP -, TN +, TN -) and the Hbridge switches (TA +, TA -, TB +, TB -) can be strategically selected based on the rated power of the inverter system in order to reduce system cost and increase efficiency. Table I shows the output voltage according to the switching states.

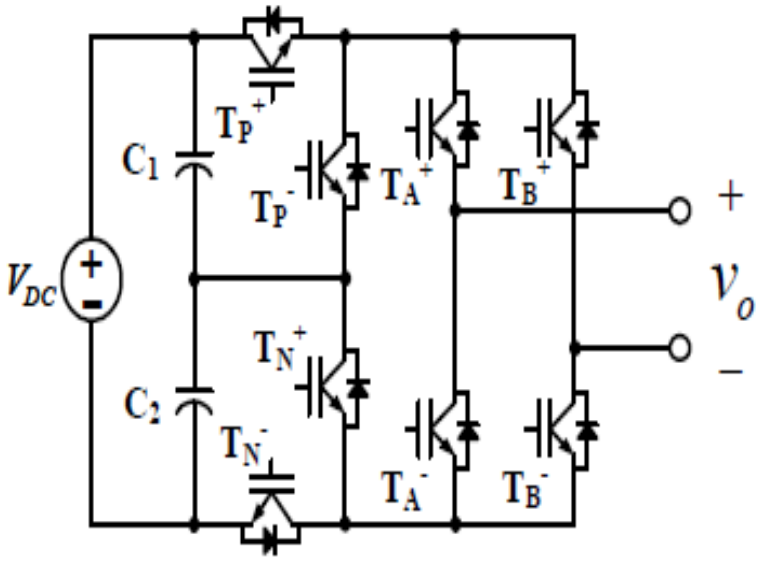

Fig. 2. Proposed single-phase multi-level inverter topology.

TABLE I
Output voltage according to switching states

Output voltage (Vo)	Switching condition					
	T_P^+	T_P^-	T_N^+	T_N^-	T_A^+, T_B^-	T_A^-, T_B^+
V_{DC}	ON	OFF	OFF	ON	ON	OFF
V_{DC} /2	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
-V_{DC} /2	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
-V_{DC}	ON	OFF	OFF	ON	OFF	ON

B. Operating modes and proposed PWM strategy

The output voltage of the proposed MLI shown in Fig. 2 has five levels (VDC, VDC/2, 0, -VDC/2, -VDC) according to the switching states of the inverter. There are four operation modes depending on the instantaneous value of the reference voltage, *v*ref and the maximum value of the carrier signal, *V*C(see Fig. 4). Table II shows the possible inverter output voltage level according to the operating mode.

In case of the N-level NPC type multi-level inverter, N-1 triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range +VDC to -VDC. A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. Three dispositions of the carrier signal are considered to generate the PWM signal [9-11].

1) Phase disposition (PD); where all carriers are in phase.
2) Alternative phase opposition disposition (APOD); where each carrier is phase shifted by 180 degree from its adjacent carrier.
3) Phase opposition disposition (POD); where the carriers above zero voltage are 180 degree out of phase with those below zero voltage.

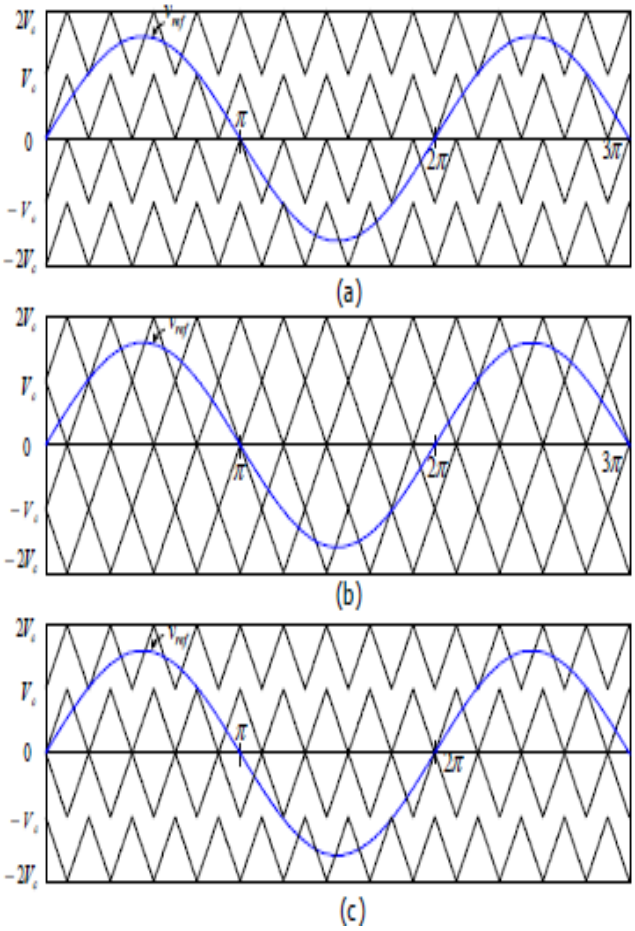

Fig. 3. Carrier and reference signal arrangements for: (a) Phase disposition (PD). (b) Alternative phase opposition disposition (APOD). (c) Phase opposition disposition (POD).

Results and Discussions

The proposed system is developed in the MATLAB/SIMULINK software. The Proposed PFC_DC Link is shown in Fig: 5.

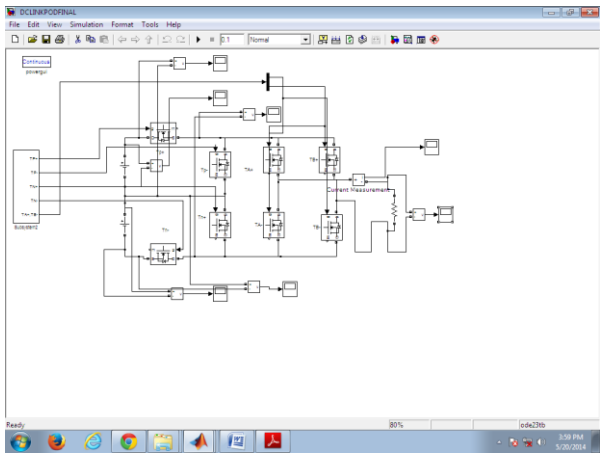

Fig: 5 Proposed PFC_DC Link Model

PFC is shown in Fig: 6, Solar Panel Modelling is shown in Fig: 7.

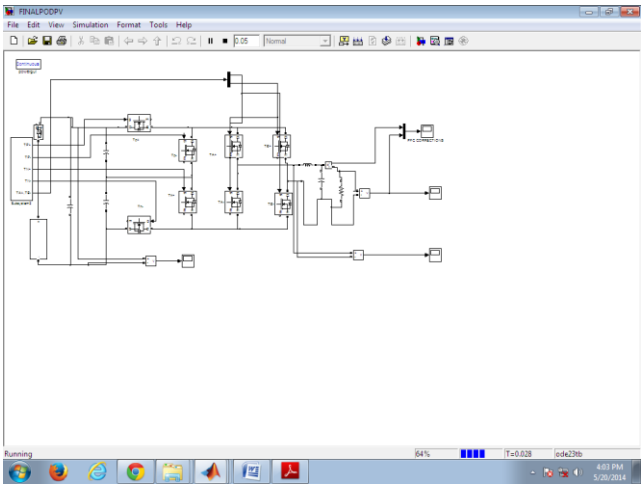

Fig: 6 PFC in MATLAB Simulink

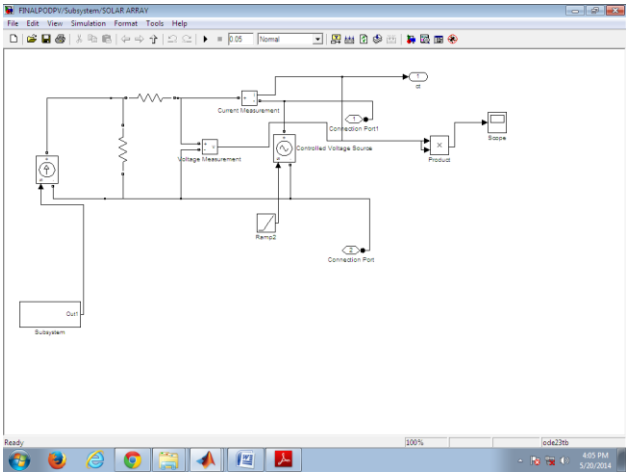

Fig: 7 Solar Modelling in Matlab

Converter Output is show in Fig: 8, AC side voltage and Currents are show in Fig: 9

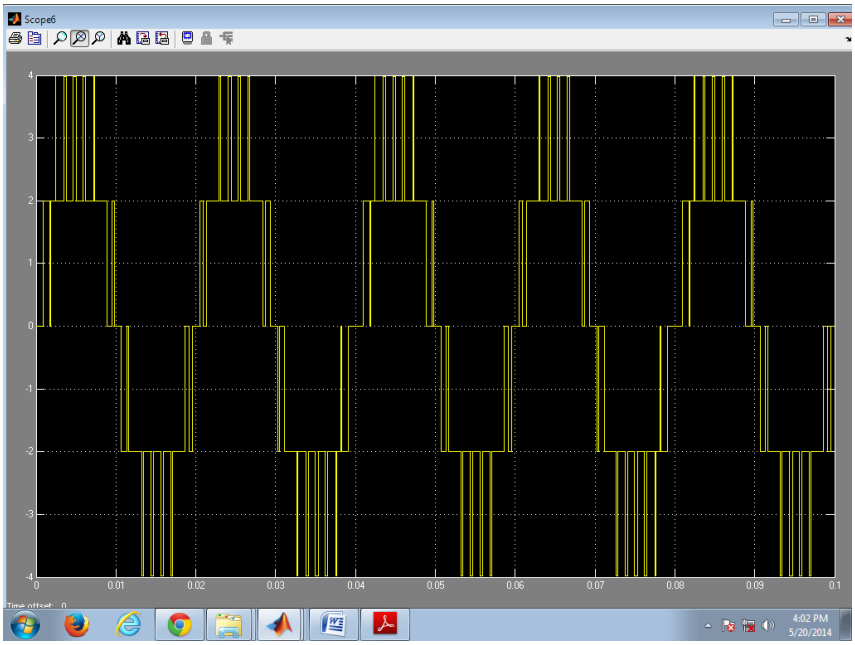

Fig: 8 Converter side output voltage

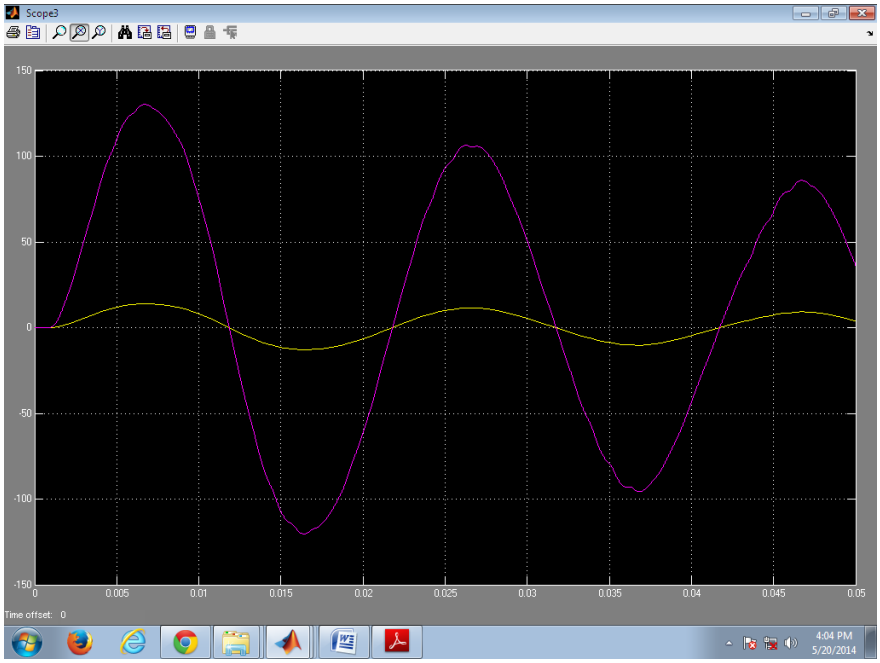

Fig: 9 AC Side output voltage and current

Conclusion

This paper proposed a new multi-level inverter topology based on a H-bridge inverter with four switches connected to the dc-link. The proposed MLI has the following advantages over the conventional inverters.

1. Number of devices of the proposed multi-level inverter is fewer than that of the conventional multi-level inverters. Therefore, the proposed system is more reliable and cost competitive than the conventional two-level and multilevel inverters.

2. The four switches (TA +, TA -, TB +, TB -) in the H-bridge are switched at a low frequency (e.g. 60 Hz). Therefore, switching loss of The four switches (TA +, TA -, TB +, TB -) is almost negligible.

3. Only one carrier signal is required to generate the PWM signals for 4 switching devices (TP +, TP -, TN +, TN -).
4. The proposed topology can be easily extended to 9-level or higher level with minimized active device component count.

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