A Review on MOSFET and its limitations: New era of transistor "FinFET Technology"

Vaishali Thakur
PG-Scholar

Prof. Pallavi Pahadiya
Professor

Dr. Akhilesh Upadhyay
Professor

Dr. Nidhi Tiwari
Associate Professor

Department of Electronics and Communication
SAGE University, Indore

Abstract: It took hundreds of years for transistors to evolve to this extent. Utmost, 1 billion transistors are scaled in a single chip, this level of growth is achieved by continuous scaling of transistors and improvements in silicon manufacturing process. FinFET is one the most promising technology today; it offers superior performance over existing planar devices due to its better electrostatics. But Si scaling in FinFET seems to be a great challenge because of narrow fin width control and power dissipation. In this paper we will discuss the barriers in this evolved leading technology and the various aspects that affect the manufacturing of it like fin shape, pitch, doping, and patterning. A major design challenge in logic and SRAM circuits that is implementation of high mobility materials is also bought in light.

Keywords: MOSFET, BJT, FinFet, DIBL, high mobility channel, gate pitch scaling,

I. INTRODUCTION

Major problem with BJT (bipolar junction transistor) was static power dissipation i.e. power is sapped even if the circuit is not switching. BJT was used over vacuum tubes. BJT was a current controlled device, a silicon piece with three regions emitter, base, collector and after this MOSFET was introduced which was current controlled device. Basic MOS transistors used metal as the gate material, silicon di oxide as insulator and semiconductor as substrate, which titled the device as MOS i.e. Metal Oxide Semiconductor Transistor, whereas FET (field effect transistor) is named because of the fact that gate switches on and off by the transistor with an electric field crossing the gate oxide. MOS transistor is 4 terminal device i.e. drain, gate, source, body. .MOS transistors can be characterized in two structures NMOS &PMOS, both of them are complimentary in nature. Generally, poly-silicon consisting of heavy doping material of either n or p type could be used as gate material, silicon is used as insulator whereas source and drain are formed by implanting donor impurities on both the sides. Allowing that two regions are biased at different potentials then the region at lower potential is source and the region at higher potential will act as drain.[1] MOS transistors are no more 'insulated gate' devices, these insulated gate were used in IGFET (insulated gate field effect transistor) or MOSFET (metal oxide semiconductor field effect transistor). IGFET and MOSFET are voltage controlled devices whose gate isolated from the body by a metal oxide layer. This layer makes the input resistance

extremely high. Simultaneously gate is electrically isolated from the main current carrying channel existing between drain and source there is no flow of current in gate. [2]

II. TECHNOLOGY SCALING

The theory of scaling was earlier given by Gordon E. Moore sir in 1965 that the number of transistors in an integrated circuit will double itself every two years, it is known as Moorey's law CMOS has better traits over NMOS with its low power dissipation, speed, packing density, performance to cost ration, improvement in processing technologies & the most important is scaling.[1] Technology scaling means the reduction of horizontal and vertical dimensions of the transistor chip along with the reduction of supply voltage VDD, which reduces power dissipation and overcome oxide breakdown. In this condition threshold voltage (Vt) is proportionally reduced to balance the output of the transistor. In contrast narrow oxide thickness and low threshold voltage gives a hike in gate leakage & sub threshold leakage currents which makes leakage power the highest contributor of the chip. Thus for the nanoscale design both dynamic and leakage power minimization are equally important. There challenge was to develop some techniques to reduce both of these components and increase battery life of the mobile components. As a result of continuous scaling the no. of dopants has reduced from thousands to few dozens, this also reduces the cost of doping that was high in CMOS devices and provided us higher functional density. New advanced technologies introduced such as double gate MOSFET, FinFET, Carbon Nanotube Field Effect Transistor are most promising and can replace classical CMOS technology.[3] Problem of planar technology was its scaling limitation was encountered in planar technology below 32 nm, so non planar designs were introduced.[1]

III. MOSFET V/s Other FET

With the Continuous scaling down of the dimensions of conventional MOSFETS to micro or nanolevel their rose a huge physical problem in conventional MOSFETS. It seems a monotonous task to upgrade the output of these devices due to the influence of short channel effect and abrupt rise in sub threshold leakage current.[1] The expanding leakage current results in power dissipation because of DIBL (Drain induced barrier lowering). In order to overcome this we have to decrease the thickness of the oxide but this increases the leakage because of GIDL (Gate induced drain leakage). To reduce the GIDL there raises a need of high and abrupt drain doping which helps reducing series resistance to attain high transistor drive current. Thus to overcome all such barriers multiple gate field effect transistors (MUGFETs) are used, types of which are FlexFET, Pi-gate FET,Tri-gate FET, FinFET. Comparatively FinFETs (double gate FET) and Gate FETs (FET with three gates) are more useful over other MUGFETs because of their simple structure and easy fabrication. Moreover FINFETs are used as an alternative to bulk MOSFETs because of their improved stability, lower leakage current, improved short channel performance and enhanced sub threshold slope. Fabrication technology of FINFET is somehow similar to MOSFETs but the double gate structures are non planar transistors in which the direction of current is parallel to the wafer and channel formed is perpendicular to the wafer.[4]

IV. PROBLEMS IN MOSFET

Channel length in MOSFET has great effect in its functioning. In case of long channel devices channel length linking the source and drain is so long whereas in short channel devices the length is short. Short channel MOS has a good processing speed and need low operating potential also improves transistor density on a single chip. With all the advantages there are some disadvantages of short channel devices. Some of them are explained in brief-

DIBL- Incase the gate voltage is more than the threshold voltage then the channel has to face the barrier that could block the flow of the charge which could be removed only after increasing gate potential. Whereas in short channel devices these potential barriers are operated by both Vgs and Vds, like if the drain voltage is raised the depletion region also enlarges in size and expands below the gate resulting in low potential barrier and flow of charge between source and drain. The concept of drain reducing the channel barrier and degrading the threshold voltage is called DIBL.

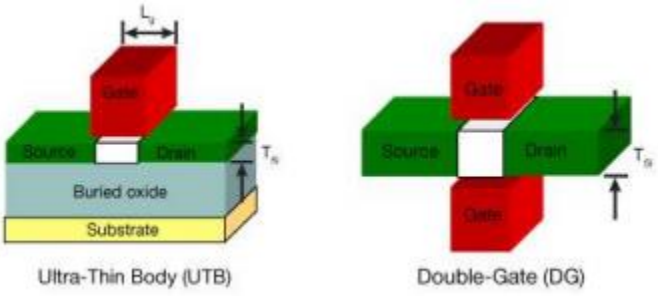
Surface scattering- In short channel devices the vertical electric field is almost negligible as compared to horizontal electric felid because of which the charged electron has to follows zig-zag path which is called as scattering. Due to this scattering effect the charge electron faces the degradation in the carrier mobility and also reduction in drain current.

Hot carrier effect- In some geometrically small size gadgets the electric field expands rapidly just about the drain which gives the carrier the ample quota of energy, these carriers are known as hot carriers. The generated hot carriers damages the oxide by tunneling through it resulting in device degradation.[1]

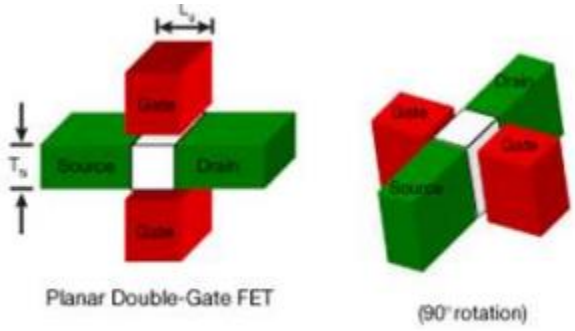
V. FinFET

According to the researches a thin structured MOSFET could control the short channel effects and restrain leakage by placing the gate capacitance nearby the channel. Keeping this in mind researchers presented 2 possible models

1. By rotating the double gate structure lowest gate leakage current could be achieved. With this gate electrodes becomes self-aligned and results in simple manufacturing using standard lithography techniques.



2. Modern FinFET are 3d structures i.e. perpendicular to the planar substrate, resulting the good control over the conducting channel by gate wrapped around the channel allowing a little amount of leakage current when in off condition.[5]



FinFET device provides better short channel control by its fully depleted behavior with the need of less or no doped channel. This les doped channel lowers the scattering of lower dopant ion resulting improved drive currents and less random dopant fluctuations (RFD). This research aims on issues raised on technology & circuit design.[6]

VI. Background and History

The research of multi gate MOSFET started centuries ago in 1980's. Hieda et al in 1987 was the first publisher of multi-gate transistor, it brought in light that fully depleted body of silicon based transistor has better switching because of low body bias effect. After 2 years DELTA- a first double gate transistor with bulk silicon was proposed by Hisamoto et al. [7] The first of its kind FinFET circuit was a four stage inverter proposed in 2002 by Rainey et al. [8]

Fin patterning and shape-

To match the essential aspects of FinFET device with the planar devices FinFETs need to be tall as per the pitch of active area which is achieved by formation two fins per minimum pitch matching the ratio with corresponding planar devices. Lithographic patterning of fins faced some issues like- to halve the minimum pitch double patterning is needed, even the buit-in overlay defect between two fin patterns could lead to undesired fin pitch variation that affects down-stream processing. This double mask layer patterning could be reduced by using SADP (self-aligned double patterning). In some cases the SADP method should be applied twice when the pitch is so small, issues caused by LER (line edge roughness) along with LWR (local fin width variability) could be easily removed by SADP. Typical method for fin patterning is when a large area of chip is patterned on single pitch only called "sea of fins" and remaining unutilized part is cut and removed this is called "fin cut". [5]

Intel has built its first 22nm node microprocessor logic product with high performance with its FinFET sidewalls sloping at 8 degrees vertical. Fins with less aspect ratio are safer and less prone to damage. Sloping sidewalls provides required trench among the fins to fill fin isolation

dielectric rather than vertical alignment. Sloping also helps improved and easy implantation of dopants in source and drain. Poor short channel control approaching the bottom of the fin raises as a disadvantage of sloped fin shape. [12, 13] This problem could be resolved by increasing doping but the negative side of sloping grows wider with scaling of gate length and the call to move towards more vertical shape arises. [6]

1. FIN dimension variability and doping

Device performance is greatly affected by fin height and width. Device's productive electrical width is directly proportional to fin height, thus any fin height disparity directly affects the device width disparity. In contrast in planar devices all fin based devices suffer equal device width error since active area patterning influences only the narrowest transistor.

In ideal state no doping should be done in a FinFET channel but to set alternate threshold voltage in determined devices and to manage under the fin leakage current some light doping is required. Implantation here proves to be the best method of doping, source and drain usually requires high doping to avoid increased series resistance. [6]

2. RELIABILITY

Finfets's fully depleted behaviour provides slashed transverse field in the device. This was invented for better NMOS reliability for dielectric breakdown (TDDB) and also for threshold voltage instability (PBTI) noticed in evolution from planar 32 nm to finfet based 22 nm technology node. PMOS reliability for both TDDB and NBTI seems unaffected for finfets [12]

3. ALTERNATIVE FIN MATERIAL-

Short channel control could be achieved in scaled finfets of about 14,10,7 nm generations but more efforts would be required to control growing power density. The most important element achieved through application of strain to channel material is increases channel carrier mobility. As the limit of silicon stressing has reached at its peak here arises a need of alternate channel material consisting of higher mobility. Search of such material is from two different families i.e. III & V material for NMOS, specifically InGaAS and Ge or SiGe with high Ge content for PMOS. Researchers have to dig more in order to get same material for both n and p type devices, additionally, majority of III-V materials possess inadequate hole mobility & Ge based solution, while expressing high electron mobility, confronts issues regarding Ge's high source and drain resistance. Silicon substrate seems as the choice of material in foreseeable future. [5]

VII. CONCLUSION

Finfet technology has proved to be a good replacement to MOSFETs. Due to its high performance this device could last for so long, whereas new fin materials are likely to be introduced in future which would even enhance its power and efficiency. Even some changes

could be expected in circuit designing since design ecosystem is swiftly maturing along with tools updates.

REFRENCES-

1. https://www.design-reuse.com/articles/41330/cmos-soi-finfet-technology-review-paper.html
2. https://ieeexplore.ieee.org/document/729736
3. https://www.researchgate.net/publication/282068481_Technology_scaling_and_its_side_effects
4. https://www.academia.edu/40263213/Simulation_study_of_Double_gate_FinFETs_using_different_HIGH-K
5. https://www.ijera.com/papers/Vol5_issue12/Part%20-%201/M512017780.pdf
6. https://www.researchgate.net/publication/261486057_FinFETs_-_Technology_and_circuit_design_challenges
7. K. Hieda et al., IEDM Tech. Dig., p. 736 (1987)
8. D. Hisamoto et al. IEDM Tech. Dig., p. 833 (1989)
9. D. Hisamoto et al. IEDM Tech. Dig., p. 1032 (1998)
10. J.-P. Colinge et al., IEDM Tech. Dig. p. 595 (1990)
11. S.-Y. Lee et al., VLSI Technol. Dig., p. 200 (2004)
12. S. Ramey, et al., IRPS (2013)