A COMPARATIVE STUDY ON THE ELECTRICAL EXECUTION OF BLG WITH THE NEARNESS IMPERFECTION

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Abstract

Think of electro liquidation as a water locked electric chair. There is no gainsaying that the electric chair in its present form needs improving. The first ever execution by electric chair, 128 years ago, on August 6, 1890 to be precise -was botched. 17 seconds after the chair's powerful electricity had coursed through the murderer's body, two doctors declared the victim dead. And then someone yelled, "Great God, he is alive!" The victim was still breathing and his heart was still beating. It took four minutes for the wife killer named Kemmler to die-and many hours for the corpse to cool off. "They could have done a better job with an axe," critics complained. However, edge roughness significantly degrades the performance of GNRFET circuits, such that its 320 times smaller energy-delay product at VDD = 0.4V increases to %10 and %40 of Si-CMOS for the roughness amplitude (ΔW WGNR) of 0.04 and 0.1, respectively.

Keywords: *power delay, performance*

Introduction:

The electro liquidation chamber will be a fireproofed Silver or gold plaited tank, with the victim restrained in copper chains/ handcuffs. Brine or saline solution fills the bath/tank which could resemble in appearance a huge bath tub, tanning booth or iron lung. Victim will be supine, head and neck out of water. The electro liquidation chamber could also resemble a glass elevator or escapologist's tank: victim placed vertically or slightly diagonally, head and neck out of water. The wet skin increases the severity of the electric shock. The bottom line is that nearly every botched electric chair execution that has ever taken place occurred because not enough electricity passed through the victim well enough and for long enough.

To develop a strategy for independently tuning ρ and n while maintaining constant d and network composition, we consider the following. First, we can target ρ by encouraging the NC network to enter – but not surpass – the initial stage of sintering. During this initial stage, grains minimize surface energy by forming necks, but otherwise grains retain their shape, and substantial grain growth does not occur (see Figure S1 in the Supporting Information). This can be accomplished by adding an annealing step before the ALD infilling which thermally activates solid state diffusion of NC atoms toward the interparticle contacts. Then, to modulate n, we can manipulate the composition of the film after ALD. Specifically, we can exploit the fact that after the NC network is infilled with Al2O3, the film still contains some

electron-trapping hydroxyl groups due to incomplete removal and/or introduction of new hydroxyls during the ALD process. Reducing the concentration of these residual traps should increase n.

Novel Channel Material CMOS: Experimental Exploration:

The experimental exploration of novel channel materials for CMOS devices is primarily motivated by their excellent transport properties. Their high room-temperature mobility's and saturation velocities are thought to be the key to the next generation ultra-fast, low power CMOS digital logic technology For long time, strain has been known to improve the channel transport properties of MOSFETs. Strained Si is the only new channel material which has recently made its way into the commercial integrated circuits. Beginning with the 90 nm technology node devices leading IC industries have incorporated strained silicon, in some form, to improve the channel transport properties Recently, substantial progress has also been made to incorporate strain in SOI 4 structures using bond-and-etch-back technique Modulations in electron and hole mobilities with the scaling of body thicknesses in strained SOI has been reported in and Also, devices fabricated on Si (110) wafer orientations has shown improved mobility characteristics over (100) devices Recently, similar results for (110) strained SOI MOSFETs has also been published Beyond silicon, germanium is an interesting candidate for Nano scale CMOS technology due to its excellent transport properties two and four times bulk mobility's for electrons and holes compared to silicon, respectively. illustrate some of the key concepts in the laser operation. Stimulated recombination of electron-hole pairs takes place in the GaAs quantum well region, where the confinement of carriers and of the optical mode enhances the interaction between carriers and radiation In particular, note the change in the electronic density of states, as a function of the "dimensionality" of the active layer, The population inversion (creation of electrons and holes) necessary for lasing occurs more efficiently as the active layer material is scaled down from bulk (3-dimensional) to quantum dots (0-dimensional). However, the advantages in operation depend not only on the absolute size of the nanostructures in the active region, but also on the uniformity of size.

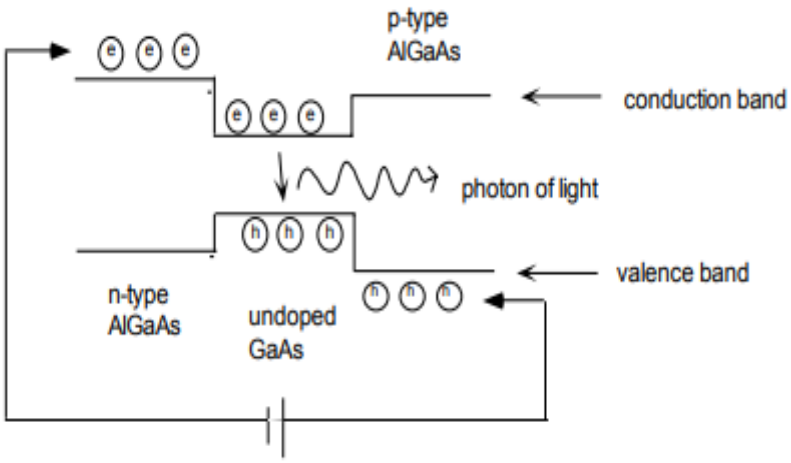


Figure shows Schematic of a semiconductor laser

Dielectrics for Ge passivation:

The poor quality Ge native dielectrics for gate insulator and field isolation have been one of the classic problems that obstruct VLSI CMOS device realization in Ge. Efforts to use materials like SiO2 on a thin Si cap, Ge3N4, GeO*x*N*y*, etc. have been only marginally successful. Inspired by the recent successes of the high-k dielectrics on Si, we investigated the possibility of applying these materials to Ge.Volatility of Ge surface oxides or sub-oxides makes surface cleaning easier for high-k gate dielectric stack free of the performance limiting, lower-k, interfacial Ge O*x* layer.

Surface passivation of Ge has been achieved with its native oxynitride (GeO*x*N*y)* and high-permittivity (high-k) metal oxides of Al, Zr and Hf. Three different techniques were studied for surface passivation: thermal growth of Ge oxynitride oxidation in ozone of metals deposited on Ge and (3) atomic layer deposition (ALD) of high-k metal oxides The oxynitride formation was studied by an initial rapid thermal oxidation (RTO) in dryO2 at 500–600 ◦C followed by *in situ* RTN at 500–700 ◦C in NH3 ambient to convert the Ge oxides into GeO*x*N*y* Optimum process temperature for both RTO and RTN was found to be 600 ◦C. The degree of nitridation in GeO *x*N*y* should be optimized for best results. Over *K.*

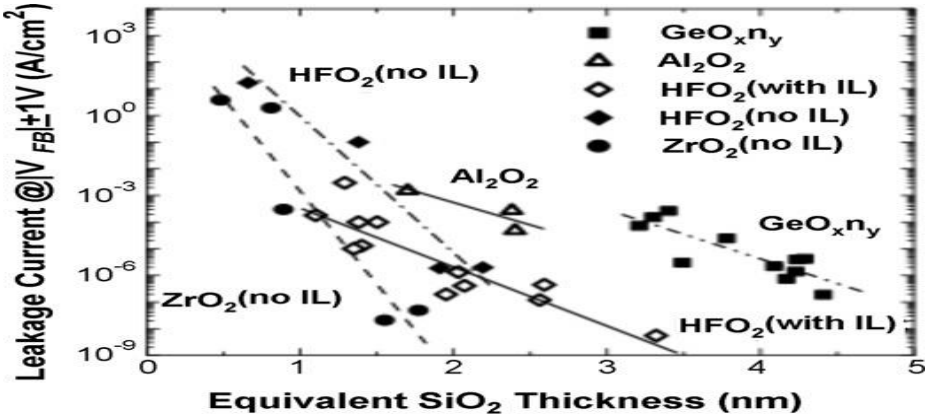


Figure shows Gate leakage measured at *V*FB + 1V vs. EOT for various dielectrics.

Nitridation led to excessive carrier generations near the nitride GeO*x*N*y*/Ge interface, increased interfacial charge trapping and positive oxide fixed charge generation, which may ultimately degrade channel mobility. This technique gave excellent *C–V* characteristics and therefore was employed to passivate the Ge surface prior to the deposition of SiO2 for field isolation.

The second technique involved UHVsputtering of∼22–30 °A Zr films on the Ge surface followed by *in situ* UV ozone oxidation at room temperature Ge/ZrO2 interface was found to be free of any significant interfacial Ge oxide with excellent *C–V* characteristics with EOT in the range of 6–10A° .In the third technique HfO2 or ZrO2 were deposited in a cold-wall high vacuum atomic-layer deposition (ALD) system at 300 ◦C, using alternating surface-saturating reactions of metal tetrachloride and H2O precursors ALD of ZrO2 films on Ge exhibited local epitaxial growth without a distinct interfaciallayer. However, *C–V* measurements showed significant *C–V* hysteresis and frequency dispersion, possibly due to metal diffusion in Ge and surface defects. To study the effect of different surface preparations prior to high-k ALD, gate leakage currents, EOTs and hysteresis from the corresponding MOSCAPs were measured. Among them cyclic rinsing between HF and H2O (CHF) for cleaning Ge and rapid thermal nitridation (RTN) in NH3 gave the best results. Conventional self-aligned process

requires high temperatures for dopant activation, imposing a thermal stability requirement on the high k gate stack.

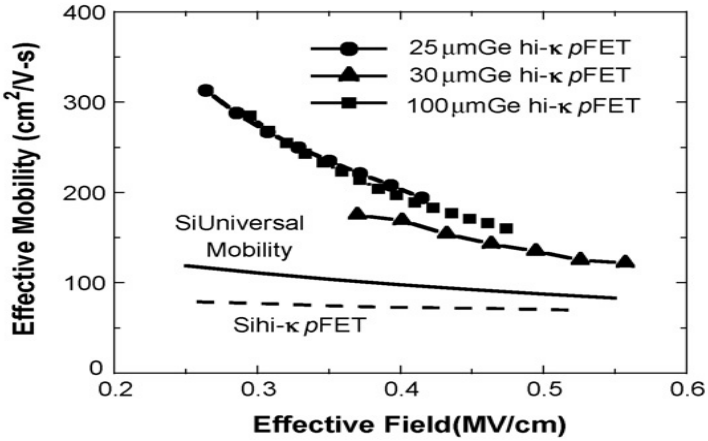
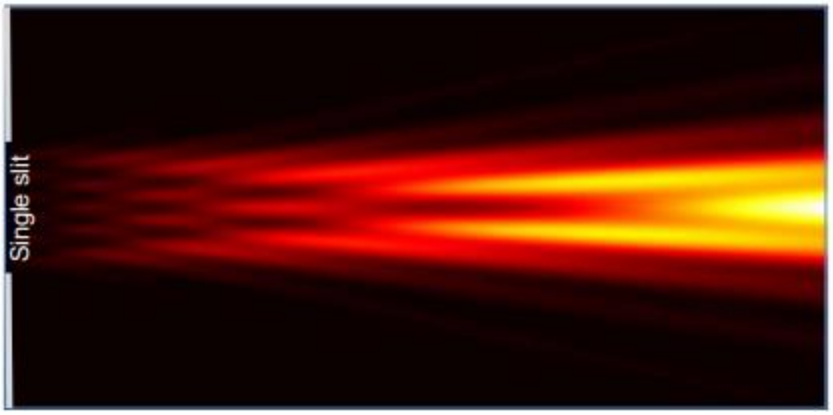


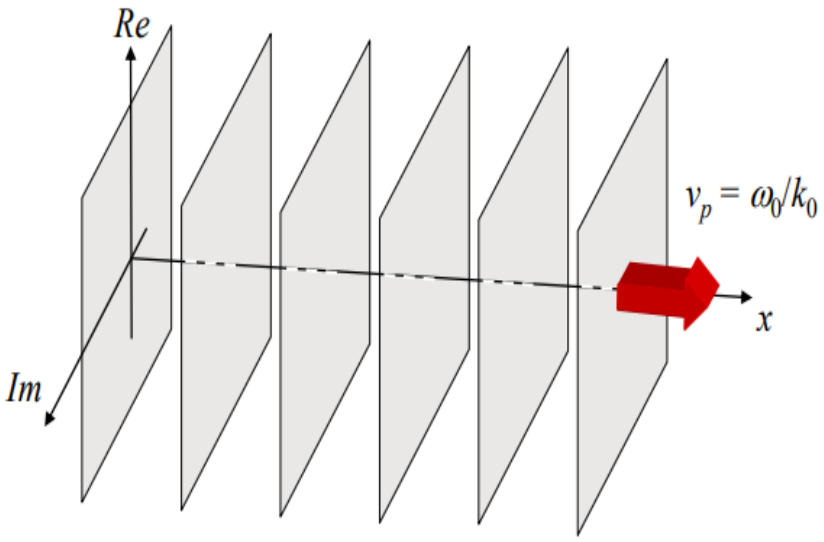
Figure Experimental hole mobility in bulk Ge p-MOSFETs

Quantum capacitance w. r. t. gate voltage:

Fig. shows that all channel materials have similar quantum capacitance verses gate voltage behavior. The device can be operated at quantum capacitance limit



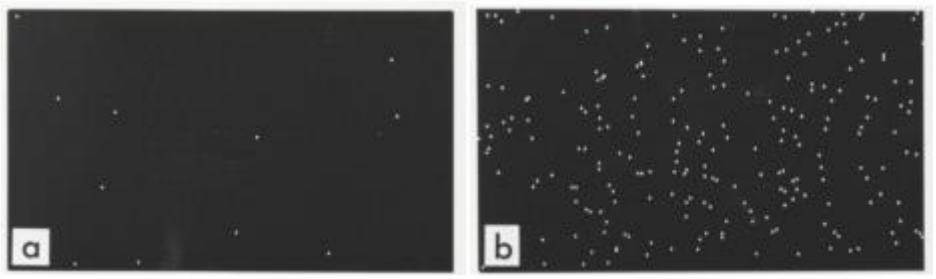
Simulation of electron diffraction through a single slit. This experiment is analyzed in Problem



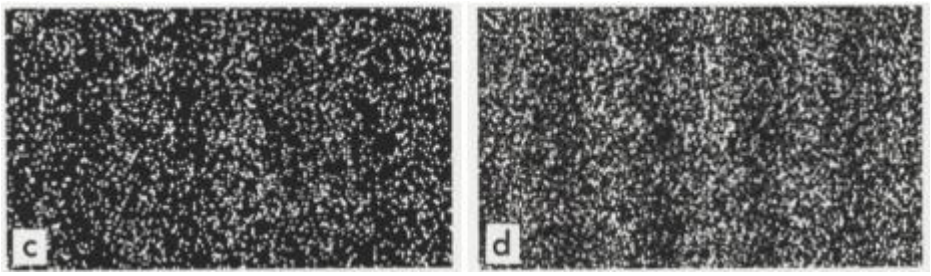
In a plane wave planes of constant phase move through space at the phase velocity

Different channel materials

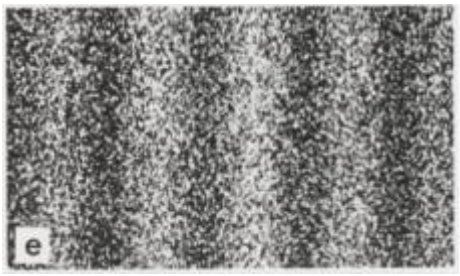
It is notable that the fringe pattern is independent of intensity. Thus, the interference effect should be observed even if just a single electron is fired at the slits at a time. For example, in Figure we show the buildup of the fringe pattern from consecutive electrons. The only conclusion is that the electron – which we are used to thinking of as a particle - also has wave properties.



10 electrons 200 electrons

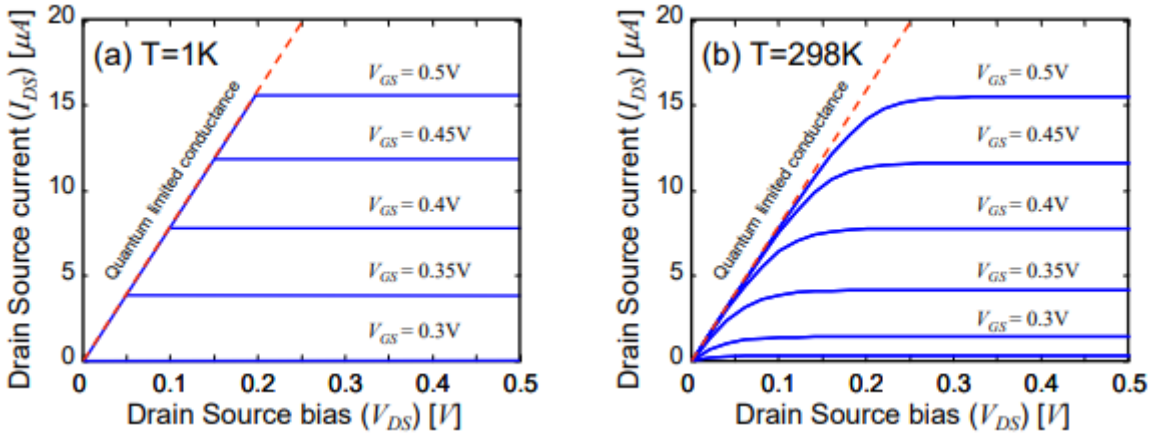


6000 electrons 40000 electrons

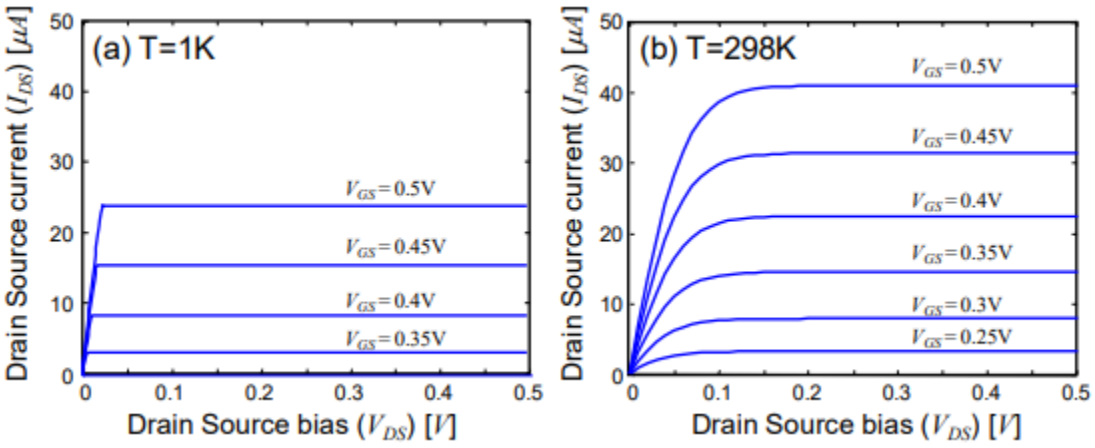


140000 electrons

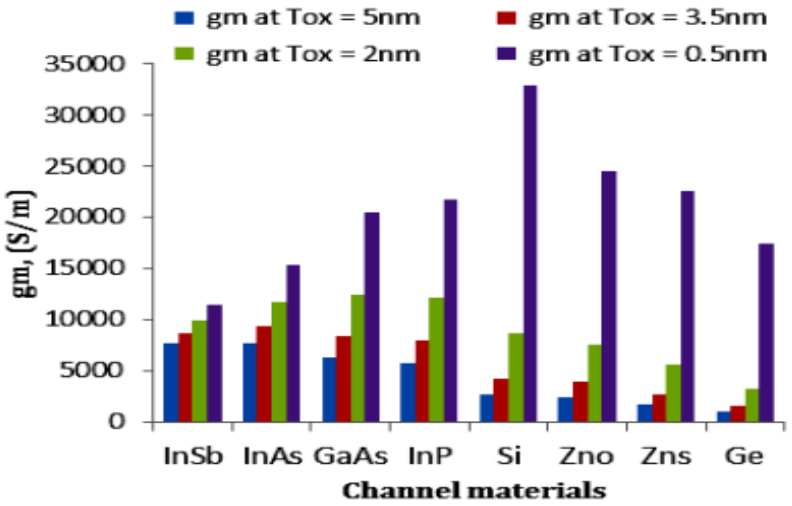
The cumulative electron distribution after passage through a double slit. Just a single electron is present in the apparatus at any time



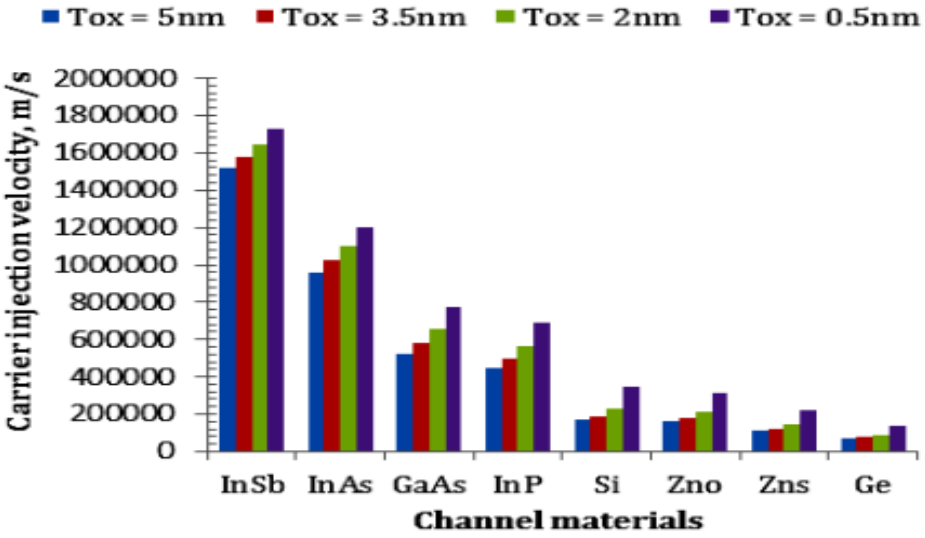
Forward bias characteristics for a quantum wire FET at (a) T = 0K, and (b) room temperature



Forward bias characteristics for a quantum well FET at (a) T = 1K, and (b) room temperature. The channel width is W = 120nm, and the electrostatic control over the channel is assumed to be idea



Graph shows Variations of Trans conductance (gm) with different channel materials at various oxide thicknesses



Graph shows Variations of Carrier injection velocity with different channel materials at various oxide thicknesses

Conclusion:

The development of interconnects and devices in nano scale regime. Therefore, researches are making an attempt to investigate such interconnects which can perform smoothly without any problem at nano scale regime and researchers have succeeded in this area they found the interconnects made up from carbon which can outperform the performance of old VLSI interconnects. In this research thesis emphasis on graphene nano ribbon has been given which has been used as an interconnect in a driver-interconnect-load circuit. In the thesis the structure of graphene nano ribbon has been discussed along with its industrial applications. Graphene nano ribbon interconnect which has been considered here is having number of graphene layers 3, 10, and 20 along with interconnect length varying from 100µm to 1000 µm and interconnect width varying from 10 nm to 50 nm. Two equivalent models of GNR have been used in this work namely single conductor and multi conductor equivalent model and also new concept of intercalated doing of GNR has been used in this work to find out the performance of the test circuits and compare it with that of neutral GNR.

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