CMOS CIRCUIT FOR OPTIMAL CURRENT BASED ON SUB THRESHOLDING

PATHLOTH KRISHNAMURTHY
ASSISTANT PROFESSOR, DEPARTMENT OF ECE,
BRILLIANT INSTITUTE OF ENGINEERING AND TECHNOLOGY, HYDERABAD.

Abstract: Till today quantities of current circuits are structured utilizing CMOS innovation among which nano control circuits are fundamental inclination because of their present reference circuit reproduction in 180nm. We propose the advancement of biasing voltage, start up supply required, current source circuits with MOSFET transistor which works in sub edge district. In which the source and door voltage VGS assumes an indispensable job. By mimicking this proposed circuit the steady reference current of few nano amperes with supply of not exactly couple of volts with affectability of 0.2V. The temperature coefficient of current is high at this voltage level, and less power dispersal at under 2V.so, proposed circuit of sub edge is utilized for VLSI CMOS circuits.

Keywords: Low voltage, Low power, Sub threshold, Temperature coefficient

Introduction: Nano ampere current references have been reported in several papers [3]-[6]. However, their power dissipation is still large, and their outputs current have a large dependence on temperature, the circuit is not enough to use as a reference current under an environment where the temperature changes because the output current that they proposed increases proportionally as the temperature increases. The purpose of this work is to offer a design method for a constant current reference circuit that works at the sub-threshold region over a large temperature range. The current reference circuit that we designed will solve these problems and can be used for ultralow-power LSIs. In digital circuits, subthreshold conduction is generally viewed as a parasitic leakage in a state that would ideally have no current. In micropower analog circuits, on the other hand, weak inversion is an efficient operating region, and subthreshold is a useful transistor mode around which circuit functions are designed. In the past, the subthreshold conduction of transistors has usually been very small in the off state, as gate voltage could be significantly below threshold; but as voltages have been scaled down with transistor size, sub threshold conduction has become a bigger factor. Indeed, leakage from all sources has increased: for a technology generation with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption. The power dissipation is few Nano watts and no resistors are used. It can provide a reference current that is insensitive to temperature and supply voltage. This paper is organized as follows: circuit configuration and operation principles, important parameters, simulation results are presented, and we conclude the paper in, Note that all the simulation. Were performed using Spectre EDA Tool in Cadence CMOS process.

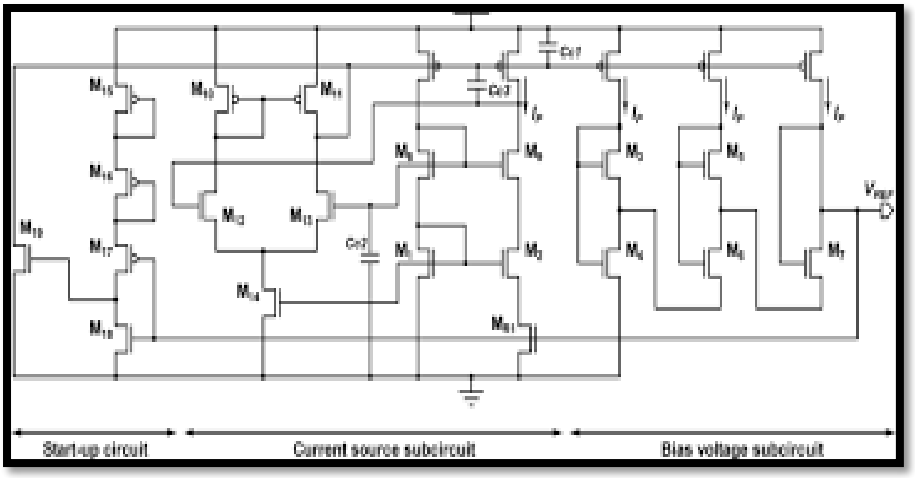

Figure.1: proposed circuit

Fig.1 shows our current reference circuit. The circuit consists of current source circuit, PTAT voltage generator, and Bias voltage circuit, start-up circuit. Sub-threshold operation achieves ultralow-power operation because the sub-threshold current is of the order of Nano- amperes. When a drain –source voltage of a MOSFET is higher than roughly 0.1 V, sub-threshold current I Is expressed as

$$\mathbf{I=KI_O \exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)}$$

Where K is the aspect ratio $(=\frac{W}{L})$ of the transistor $\mathbf{I_O} = (=\mu C_{ox}(n-1)V_T^2)$ is a process dependent parameter, μ is the carrier mobility, $C_{ox}(=\frac{\varepsilon_{ox}}{t_{ox}})$ is the gate-oxide capacitance, is the oxide permittivity, is the oxide thickness, is the sub-threshold slope factor, is the a gate-source voltage, $v_T(=\frac{K_B T}{q})$ is the threshold voltage, is the Boltzmann constant , T is the absolute temperature, q is the elementary charge, and is the threshold voltage of the MOSFET. We will use (1) to analyze the characteristics of a sub-threshold MOSFET. Note that, in this work, we assumed that is a constant parameter (in the process used, ~1.14 and 1.40 for n MOSFETs and p MOSFETs, respectively). However, is not constant in actual devices and depends on the gate-oxide and depletion –layer capacitances. The circuit consists of a current source circuit. All the MOSFETs operate in the sub-threshold region except for the MOS resistor ( ) that operates in the strong-inversion and deep triode regions. This circuit has two advantages compared with the basic β multiplier [1]: the first is that it needs No resistor of high resistance that occupies a large area on an LSI chip, and the second is that it can achieve a zero temperature coefficient of Current for an appropriate bias voltage for the MOS resistor.

PTAT Voltage Generator: The MOS divider in Fig. 1 is well known for its PTAT output when both transistors operate in weak inversion [3]. The result has recently been extended to strong inversion when the bias current has special temperature dependence [4]. In this section we show that the MOS divider output is PTAT for any inversion range, including moderate inversion, when biased by a current in such a way that the inversion level remains constant over temperature. We will first review a couple of general expressions that will be used later on. The

PTAT voltage generator consists of a differential pair with a current mirror. When the MOSFETs operate in the sub- threshold region, gate to gate voltage in this circuit can be expressed from (1) as

$$\mathbf{V_{GG} = nV_T \ln(\frac{k_{d1}k_{M2}}{k_{d2}k_{M1}})}$$

Where and correspond to aspect ratios in the differential pair, and corresponds to aspect ratios in the pMOS- current mirror. Therefore, PTAT voltage can be generated by making $\frac{k_{d1}k_{M2}}{k_{d2}k_{M1}} > 1$ the characteristic of MOS resistor is controlled by the bias voltage sub- circuit. The diode connected MOS generate the voltage for and in the voltage generator circuit, which set up the gate to source voltage of for operating in the strong-inversion and deep-triode region. The current flowing in the circuit is determined by the characteristics of PMOS M_R resistor that is operating in deep-triode region. If $V_{GSR} > V_{TH} > V_{DSR}$ the current is given by

$$\mathbf{I_{REF} = \mu C_{ox} K_R (V_{GSR} - V_{TH}) V_{DSR}}$$

The gate length L and the gate width W of and are the same and they are biased at the same current. The PTAT voltage generator adds a voltage to the gate-source voltage of in order to increase that of .The difference in their gate-source voltages forced across MOS resistor .Equally sized MOSFETs and make their threshold voltage similar, so the value of the generated current is robust to process variations. A start-up circuit is required to avoid the stable state in the zero bias condition.

IMPORTANT PARAMETERS

Temperature coefficient: Temperature coefficient (TC) is a measure of the output current change with respect to change in the operating temperature. The TC of the output current given by

$$\mathbf{TC=\frac{1}{I_{REF}}\frac{dI_{REF}}{dT}}$$

Line sensitivity: Line sensitivity is a measure of the circuit ability to maintain the specified output current with varying supply voltage.

$$\mathbf{L.S=\frac{\Delta I_{REF}}{\Delta V_{DD} I_{REF}} * 100}$$

Load regulation: Load regulation is a measure of the circuit Ability to maintain the specified output Current under the load varying condition.

$$\mathbf{L.R=\frac{I_{no\ Load} - I_{Max\ Laod}}{I_{Max\ Load}} * 100}$$

Power supply rejection ratio: It is the ability of the circuit to reject the noise present in supply voltage at different frequencies. PSRR should be high for better circuit performance.

$$\mathbf{PSRR=20\ log_{10}\frac{output\ ripple\ voltage}{input\ ripple\ voltage}}$$

SIMULATION RESULTS: The simulation of the circuit was done in cadence EDA tool in 180 nm CMOS process by using Spectra for schematic analysis and virtuoso for layout analysis at room temperature. For circuit simulation we use the ADE window for different type analysis of the circuit, like DC, AC, Trans, parametric, corner, Monte- Carlo etc. For that circuit I was performed DC analysis for calculation of reference output current.

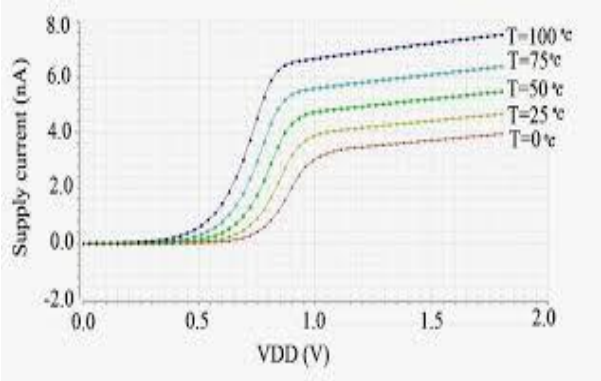

Figure.2: output current at room temperature

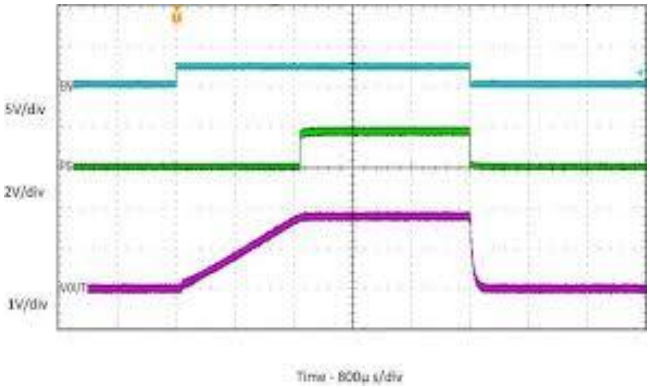

Figure.3: output current I_{REF} as a function of temperature

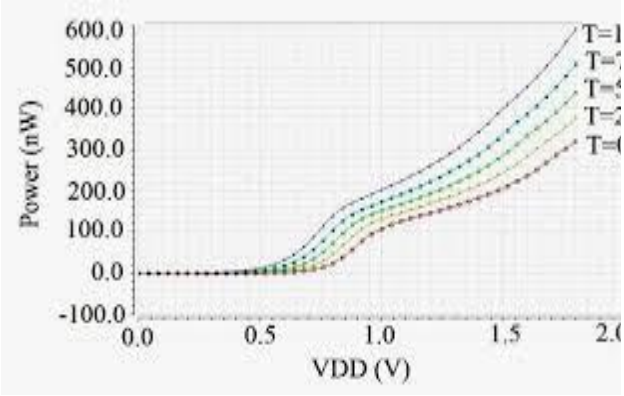

Figure.4: DC power as a function of supply voltage for different value of temperature.

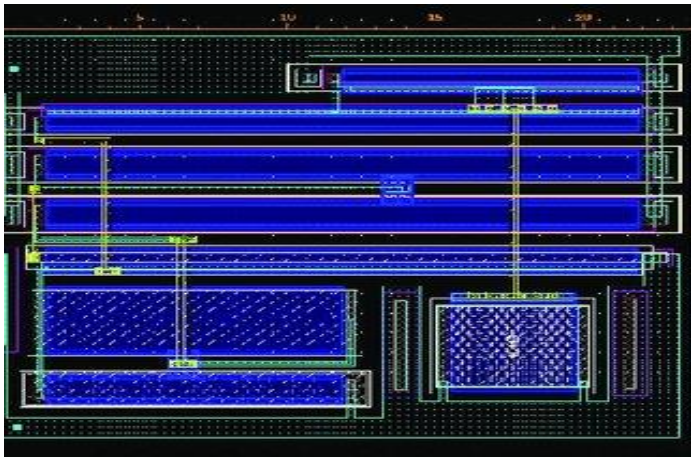

Figure.5: proposed design layout

Fig.1 represents generated reference current as a variation of operating voltage at absolute temperature. The designed circuit will work accurately when the operating voltage is greater than 1 V. The line sensitivity is in an operating voltage range of 1 to 1.8V .This circuit has the capability to produce a Nano ampere output current it mostly independent on the operating voltage and temperature.Fig.2 shows generated constant output current against the variation of operating temperature for a 1.8V operating voltage for temperature range 0c-100c. The TC at supply voltage 1.8 V was 7529ppm/c. Fig. 3 shows the generated constant output current against the variation of operating voltage in range 1 to 1.8 V for different value of temperature in range o0to 100c. Fig.4 shows the DC power of the circuit at supply voltage 1.8V for different value of operating temperature.

Parameters	Ref. [3]	Ref. [4]	Ref. [5]	Ref. [6]	This work
CMOS technology	1.5µm	3µm	2µm	2µm	0.18µm
V_{DD}(V)	1.1	3.5	1.2	5	1-1.8
I_{REF} (nA)	.41	774	1-100	285	4
TC pmm/^{0}C	2500	375	1100	230	7592
LS%	6	0.015	10	-	0.203
TEMP/^{0}C	-20 to 70	0 to 80	-40to 80	0 to 75	0 to 100
Power (μW)	0.002	10	.07	-	0.38
Die area(mm)^2	0.046	0.2	.06	-	0.0306

CONCLUSION: In this work implements a Nano-ampere reference current generator circuit. Which can operate at a wide range of supply voltage, and the performance was simulated in 180 –nm CMOS process. The designed circuit generates a constant reference current of 4 nA .The line regulation is 0.203%/V in operating voltage range of 1 to 1.8 V. The TC was 7592ppm/^{o}C. The power consumption of the circuit about 380nW at 1.8 V supply. In future, we are working towards further reduction of the temperature coefficient, power dissipation and improvement of line regulation by using current trimming techniques and other new MOS structure.

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