CMOS/VLSI TECHNOLOGY BASED POWER CONSUMPTION OPTIMIZATION CHALLENGES

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Abstract: Now days electronic assumes a crucial job in advanced world in, which each versatile electronic gadget is basic in human life yet control utilization of those gadgets, is a noteworthy issue for which numbers of CMOS/VLSI innovations are created to beat it. In this paper control dispersal is focused which has moved toward becoming as critical thought as execution and region. This power utilization can likewise be found in remote, optical and numerous other correspondence innovations which can cause an information misfortune. Consequently, to have extremely low power utilization, this examination work is chosen to think about utilizing CMOS/VLSI innovation, and we see the impediments in this field.

Keywords: Submicron, Low Power Consumption, Paradigm Shift.

Introduction: In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth; this is because of the use of integrated circuits in computing, telecommunications and consumer electronics. The major concern of VLSI designer were area, performance, cost and reliability, power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like to low power, reliable performance and improvements in the processing technology. Scaling of technology node increases power-density more than expected. CMOS technology beyond 65 nm node represents a real challenge for any sort of voltage and frequency scaling starting from 120 nm node, each new process has inherently higher dynamic and leakage current density with minimal improvement in speed. Between 90 nm and 65 nm, the dynamic power dissipation is almost same whereas there is ~5% higher leakage/mm2. Low cost always continues to drive higher levels of integration, whereas low cost technological breakthroughs to keep power under control are getting very scarce. Modern System-on-Chip demand more power. In both logic and memory, static power is increasing really fast and dynamic power is also rising. Overall power is dramatically increasing. If the semiconductor integration continues to follow Moore's Law, the power density inside the chips will reach far higher than the rocket nozzle. Power dissipation is the main constrain when it comes to portability. The mobile device consumer demands more features and extended battery life at a lower cost. About 70% of users demand longer talk and stand-by time as primary mobile phone feature. Top 3G requirement for operators is power efficiency. Customers want smaller and sleeker mobile devices. This requires high levels of silicon integration in advanced processes, but advanced processes have inherently higher leakage current. So there is a need to bother more on reducing leakage current to reduce power consumption. Power Management matter in System on Chip due to following concerns

Sources of Power Dissipation: The power dissipation in circuit can be classified into three categories as described below. Dynamic power consumption: Due to logic transitions causing logic gates to charge/discharge load capacitance.

Short-circuit current: In a CMOS logic P-branch and N-branch are momentarily shorted as logic gate changes state resulting in short circuit power dissipation.

Leakage current: This is the power dissipation that occurs when the system is in standby mode or not powered. There are many sources of leakage current in MOSFET. Diode leakages around transistors and n-wells, Sub threshold Leakage, Gate Leakage, Tunnel Currents etc. Increasing 20 times for each new fabrication technology. Insignificant issues are becoming dominating factors.

Low-Power Design Techniques: An integrated low power methodology requires optimization at all design abstraction layers as mentioned below.

VLSI circuit design for low power: The growing market of portables such as cellular phones, gaming consoles and battery-powered electronic systems demands microelectronic circuits design with ultra low power dissipation. As the integration, size, and complexity of the chips continue to increase, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits. As the technology node scales down to 65nm, there is not much increase in dynamic power dissipation. However the static or leakage power reaches or exceeds the dynamic power levels beyond 65nm technology node. Hence the techniques to reduce power dissipation are not limited to dynamic power. In this article we discuss circuit and logic design approaches to minimize dynamic, leakage and short circuit power dissipation. Power optimization in a processor can be achieved at various abstract levels. System/Algorithm/Architecture has a large potential for power saving even these techniques tend to saturate as we integrate more functionality on an IC. So optimization at Circuit and Technology level is also very important for miniaturization of ICs. Total Power dissipated in a CMOS circuit is sum of dynamic power, short circuit power and static or leakage power. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product. In the sections to follow we summarize the most widely used circuit techniques to reduce each of these components of power in a standard CMOS design.

$$P_{total} = C_L VDD2 + tscVDDI_{peak} + VDDI_{leakage}$$

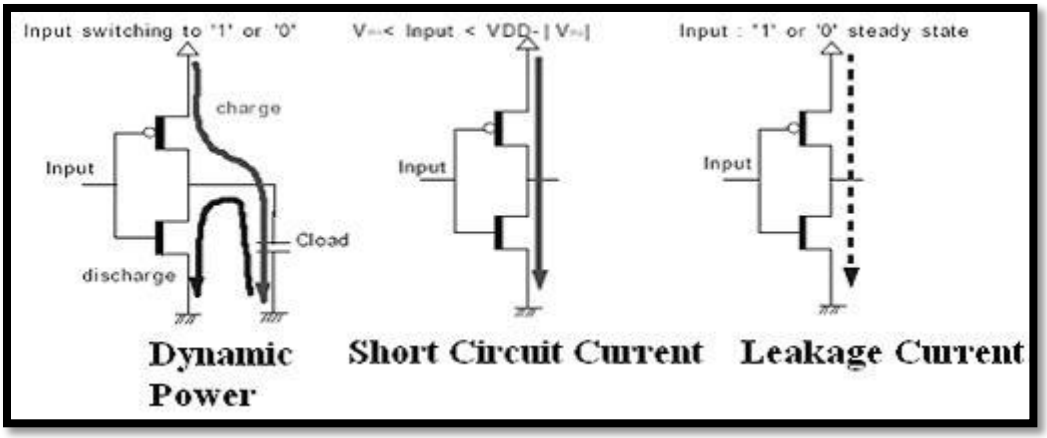

Figure 1: Components of Power in CMOS circuit

Low Power Consumption: There are various interpretations of the Moore's Law that predicts the growth rate of integrated circuits. One estimate places the rate at 2X for every eighteen months. Others claim that the device density increases ten-fold every seven years. Regardless of

the exact numbers, everyone agrees that the growth rate is rapid with no signs of slowing down. New generations of processing technology are being developed while present generation devices are at very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then come's the Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2.40 GHz [1]. While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size of the integrated circuits. If this exponential rise in the power density were to increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electro migration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance.

Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power. A study by American Council for an Energy-Efficient Economy estimated that office equipment account for 5% for the total US commercial energy usage in 1997 and could rise to 10% by the year 2004 if no actions are taken to prevent the trend [2]. The increasing prominence of portable systems and the need to limit power consumption (and hence, heat dissipation) in very-high density ULSI chips have led to rapid and innovative developments in low-power design during the recent years. The driving forces behind these developments are portable applications requiring low power dissipation and high throughput, such as notebook computers, portable communication devices and personal digital assistants (PDAs).In most of these cases, the requirements of low power consumption must be met along with equally demanding goals of high chip density and high throughput. Hence, low-power design of digital integrated circuits has emerged as a very active and rapidly developing field of CMOS design. There is a close correlation between the peak power dissipation of digital circuits and reliability problems such as electro migration and hot-carrier induced device degradation. Also, the thermal stress caused by heat dissipation on chip is a major reliability concern. Consequently, the reduction of power consumption is also crucial for reliability enhancement. The methodologies which are used to achieve low power consumption in digital systems span a wide range, from device/process level to algorithm level. Device characteristics (e.g., threshold voltage), device geometries and interconnect properties are significant factors in lowering the power consumption. Circuit-level measures such as the proper choice of circuit design styles, reduction of the voltage swing and clocking strategies can be used to reduce power dissipation at the transistor level. Architecture-level measures include smart power management of various system blocks, utilization of pipelining and parallelism, and

design of bus structures. Finally, the power consumed by the system can be reduced by a proper selection of the data processing algorithms, specifically to minimize the number of switching events for a given task.

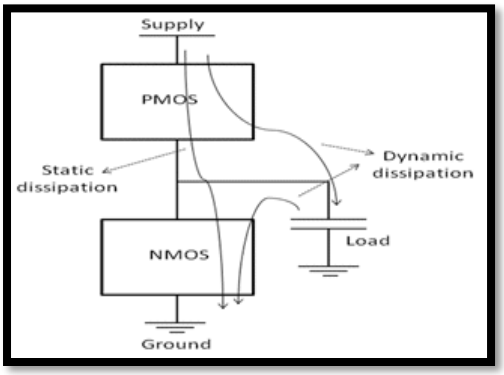

Figure.2: low power utilization circuit

CMOS Technology: The evolution of important parameter such as integrated circuit (IC) complexity, gate length, switching delay, supply voltage with a prospective vision down to the 11 nm CMOS technology. The naming of the technology nodes (130, 90, 65, 32, 22, 16, 11 nm) comes from the International Roadmap for semiconductors [ITRS2009]. The trends of CMOS technology improvement continues to be driven by the need to Integrate more functions within a given silicon area Reduce Fabrication cost To increase operating speed Dissipate less power Table 1 gives an overview of the key parameters for technological nodes from 130 nm, introduced in 2001, down to 11 nm, which is supposed to be in production in the 2015-2018 timeframe [3] [4].

Table. 1: Technological evolution and forecast

Technology node	130nm	90nm	65nm	45nm	32nm	22nm	16nm	11nm
First production	2001	2003	2005	2007	2009	2011	2013	2015
Effective gate length	70nm	50nm	35nm	30nm	25nm	18nm	12nm	9nm
Gate material	Poly	Poly	Poly	Metal	Metal	Metal	Dual?	Triple?
Gate dielectric	SiO_2	SiO_2	SiON	High K	High K	High K	High K	High K
Raw Mgates/mm^2	0.25	0.4	0.8	1.5	2.8	5.2	9.0	16.0
Memory point(μ^2)	2.4	1.3	0.6	0.3	0.17	0.10	0.06	0.06

Sub-Micron CMOS Technology Limitations: In order to design a CMOS PA, one must first understand the limitations of submicron CMOS technology with respect to PA implementations. Low breakdown voltages, low transconductance-to-current ratio, and low substrate resistivity, as will be discussed successively.

Low Breakdown Voltages: The gate oxide breakdown occurs when the electric field in the oxide exceeds a certain value (about 0.07 V/°A in silicon dioxide). This process is destructive to the transistor because it results in a permanent short circuit between the gate and the channel. As the gate length in a CMOS technology shrinks, so does the thickness of gate oxide to avoid short channel effects [6]. Thus, the maximum allowable gate voltage for a sub- micron CMOS device is greatly limited. In addition to gate oxide breakdown, the drain-substrate pn junction will conduct a large current if the reverse bias applied to it exceeds a certain value [6]. This breakdown is nondestructive, but limits the maximum PA voltage swing at the drain of the

device.

Low Tran's conductance-to-current Ratio: When the velocity saturates, the ratio of the transconductance to the current for a short-channel MOS device is [7]

$$\frac{g_m}{I} = \frac{1}{V_{GS-}V_T} = \frac{1}{V_{ov}}$$

For a bipolar device, this ratio is $1=V_T$, where the thermal voltage V_T is 26 mV. In contrast, the overdrive V_{ov} for MOS transistors is typically chosen as several hundred mV. Thus, the transconductance per given current is much lower for MOS devices than for bipolar devices. To accommodate this small transconductance, either the input signal amplitude or the device size of the PA output stage has to be increased. However, either approach will increase the loading for the driving stage, thus resulting in higher power consumption of the driver stage. Increasing the input signal amplitude can also dramatically degrade the PA linearity because the third-order nonlinearity of the device current is directly proportional to the cube of the input voltage amplitude. Thus, higher nonlinearity will be expected for MOS devices than for bipolar devices.

Low Substrate Resistivity: In an integrated implementation, a PA resides on the same substrate as other circuit blocks, some of which may be very sensitive. Since many CMOS processes use low resistivity substrates, PA signals can be easily conducted across long chip distance to corrupt adjacent circuit blocks. Thus, substrate isolation is a crucial design issue for integrated PA implementations. In addition, a low-resistivity substrate has a detrimental effect on spiral inductors built above it [8].

Conclusion: The basic theory of Low Power Design along with various Limitations has been discussed This paper has illustrated the significance of Low Power design in the communication and the trends in CMOS Technology based on technology information available from integrated manufacturers. This article reviews various strategies for designing low power circuit and system. The article concludes with the future challenges that must be met to design low power, high performance systems.

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