PERFORMANCE EVALUATION OF BRENT KUNG ADDER USING NEURAL NETWORKS

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ABSTRACT: Artificial neural networks can achieve high computation rates capable of exploiting fine grained parallelism. This paper addresses the issue of multiple valued logic, Brent Kung adder, and the artificial neural network is proposed. The neural network brent kung adder can be trained based on the traditional back-propagation learning algorithm, thus, permitting a multiple-valued logic neural network with supervised learning capability. A single neural network Brent Kung adder model for the binary, systems is also designed. It is proved that the resulting new model functions correctly with different radices. The neural network Brent kung adder is characterized by its design simplicity, its unification of different radices, and its suitability for digital applications. From the VLSI point of view, the hardware implementations are very simple and straightforward.

KEY WORDS: Neural network, Brent kung adder, VLSI.

I.INTRODUCTION

Artificial neural networks are motivated by biological nervous systems. Modern computers and algorithmic computations are good at well-defined tasks. Biological brains, on the other hand, easily solved speech and vision problems under a wide range of conditions are considered tasks that no digital computer has solved adequately. This inadequacy has prompted researches to study biological neural systems in an attempt to design computational systems with brain-like capabilities. At the same time, modern analog and digital integrated circuit technologies are offering the potential for implementing massively parallel networks of simple processing elements.

Neuro computing will enable us to take advantage of these advances in VLSI by providing the computational model necessary to program and coordinate the behavior of thousands of processing elements. Neural network models are providing new approaches to problem solving. Neural networks can be simulated on special purpose, neural hardware accelerators as well as conventional machines. For maximum processing speed they may even be realized using optical implementations or silicon VLSI. The key to the utility of artificial neural networks is that they provide a computational model that can be used to systemize the process of programming an ultra-fine-grained parallel computer with a massive number of simple processors.

Addition operation is the main operation in digital signal processing and control systems. The fast and accuracy of a processor or system depends on the adder performance. In general purpose processors and DSP processors the addition operation addresses are taken from simple Ripple Carry Adder. It is used for the addition operation i.e., if N-Bits addition operation is performed by the N-Bit Full Adder. In Ripple Carry Adder each Bit Full Adder operation consists of sum and carry that carry will be given to next Bit Full Adder operation, that process is continuous till the N^{th} bit operation. The N-1^{th}Bit Full Adder operation carry will be given to the N^{th}Bit Full Adder operation present in the Ripple Carry Adder

The design of a high-speed multi operand adder called Parallel Prefix Adders. The Prefix outcome of the operation depends on the initial inputs. The Parallel involves the execution of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel. This operator is associative hence it can be implemented in a parallel fashion. Different topologies for the parallel generation of carries. Adders that use these topologies are called Parallel Prefix Adders.

Parallel algorithms for prefix sums can often be generalized to other scan operations on associative binary operations and they can also be computed efficiently on modern parallel hardware. Many parallel implementations follow a two pass procedure where partial prefix sums are calculated in the first pass on each processing unit; the prefix sum of these partial sums is then calculated and broadcast back to the processing units for a second pass using the now known prefix as the initial value. Asymptotically this method takes approximately two read operations and one write operation per item.

. The development of multiple-valued logic algebra has proceeded since the pioneering papers of Lukasiewicz. Since then, there have been many multiple-valued logic algebra developed, and several applications for image processing networks and knowledge information processing systems presented. The most pressing problems in present binary VLSI circuits are interconnection problems. Motivated by these, there is much research of VLSI circuits based on multiple-valued logic because this latter has the power to increase the information content of the digital signals in a system to a higher value than that provided by binary operations, where the VLSI interconnection problems can be solved.

The traditional back-propagation learning algorithm can be borrowed to train the neuro-algebra based on multiple-valued logic networks directly, thus, permitting a multiple valued logic network with supervised learning capability. This research also studies the design of a single artificial neural network model for half adders of binary, ternary, quaternary and quinary systems. The model has proven its efficiency with these four different radices. Not to forget the simplicity of the hardware implementation due to the design simplicity of the network. The advantages of the proposed neural network Brent kung adder adder model are resumed to: one network covers four adder models, high performance, and suitability for digital applications with highly parallelism. Moreover, other advantages of the proposed artificial neural network are mathematical characteristics that allow simple realization, and the parameters (synapses' weights and thresholds) that fit digital applications, which ease network optimization and hardware design.

II. RELATED WORK

Artificial neural networks have been studied for more than 40 years. There has been a major resurgence of interest in neural networks in recent years, primarily because of improved learning algorithms, improved theoretical foundations, greatly improved computer systems for simulation studies, and improved implementation technologies. Artificial neural networks can achieve high computation rates by employing a massive number of simple processing elements with high degree of connectivity between the elements. Neural network connections provide a computing model capable of exploiting fine-grained parallelism.

Traditionally, VLSI circuits at gate-level were represented by binary system. This is used to be very successful for combinational

circuit, knowing the input-output of a combinational network. Although the corresponding network design is easily obtained, it is not necessary the optimal network. So far, the learning capability of the most promising multiple-valued logic networks synthesized on the currently available algebra has restricted potentials. The learning capability of a network is very important in many applications such as image processing, speech recognition and digital systems.

The weighted inputs to a neuron are accumulated and then passed to an activation function which determines the neuron response. Commonly, a continuously varying, sigmoid activation function is used to model the frequency modulated, and the action potential output of a biological neuron. The output of the model neuron ranges between limits, such as 0 and 1, that are analogous to a biological neuron's minimum and maximum firing rates, respectively. When an artificial neuron's output is 0, the model neuron is said to be "off" (or in state 0); the neuron is said to be "on" (or in state 1) if its output is 1.

A new arithmetic multiple-valued logic is introduced. It is called neuro-algebra for it has very similar formula and architecture to neural networks. The neuro-algebra deals with finite sets of values. In Kleen's regularity, 0 (false) and 1 (true) are identical with the standard truth values in binary logic. There are many researches of multiple-valued logic functions which are extensions of studies on regular binary logic functions. To design highly parallel digital circuits such as adders, it is difficult to find the optimal digital system. On the other hand, the use of neural networks seems to be very attractive to achieve highly parallel digital circuits.

III. PROPOSED SYSTEM

The Proposed Brent Kung parallel prefix adder is flexible to speed up the binary addition and the structure looks like tree structure for the high performance of arithmetic operations. In Ripple Carry Adders each bit wait for the last bit operation. In Parallel Prefix Adders instead of waiting for the carry propagation of the first addition, the idea here is to overlap the carry propagation of the first addition with the computation in the second addition, and so forth, since repetitive additions will be performed by a multi operand adder.

Research on binary operation elements and motivation gives development of devices. Field programmable Gate arrays [FPGA's] are most popular in recent years because they improve the speed of microprocessor based applications like mobile DSP and telecommunication. The construction of Efficient Ladner-Fischer Adder consists of three stages. They are Pre-Processing Stage, Carry Generation Stage, and Post-Processing Stage. The first input bits goes under Pre-Processing Stage and it will produce propagate and generate. These propagates and generates undergoes Carry Generation Stage produces carry generates and carry propagates, these undergoes Post-Processing Stage and gives final sum. From below figure (1) we can observe the proposed system block diagram.

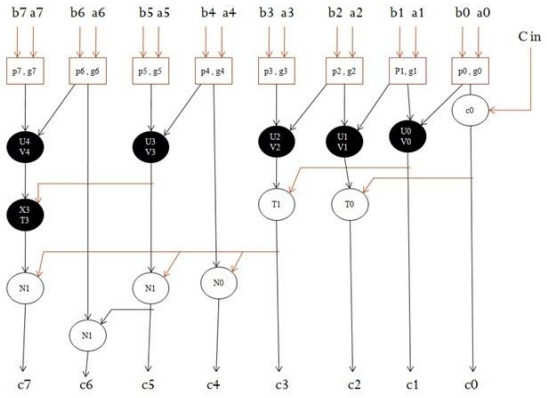

Fig. 1 proposed system

The Efficient Brent Kung parallel prefix Adder structure is looking like tree structure for the high performance of arithmetic operations and it is the fastest adder which focuses on gate level logic. It designs with less number of gates. So, it decreases the delay and memory used in this architecture. In Efficient Ladner-Fischer Adder, black cell operates three Gates and gray cell operates two Gates. The gray cell reduces the delay and memory because it operates only two Gates. The Proposed Adder is design with the both black and gray cells. By using gray cell operations at the last stage of Proposed Adder gives an enormous dropping delay and memory used.

BK Adder is a multi-bit carry-propagate adder which is used for parallel sum of two multi-bit numbers. BK extend the generated and propagated logic of the carry look-ahead adder to perform addition even faster. BK adder consists of three stages. They are pre-processing stage, carry generation stage and post processing stage. In pre-processing stage, the generate and propagate signals are carried out. In carry generation stage prefix graphs are used to define the tree structure. At last in post processing stage, sum and carry is calculated.

In the stage of prefix computation, the carries are grouped according to the adder's configuration regarding lower cost, power, and delay. According to the adder's configuration, the prefix computation groups both values directly from the input with values that were computed in the pre-processing stage. The increased delay is obtained by the configuration that has the highest critical path like the adders which process more than two inputs.

In the post-processing stage, the carry values that compose the output, are grouped. They are reached through the last adder configuration that is arranged by a solution that solves the problem of the correct carry propagation for each input bit. The final sum configuration is structured by an XOR function that captures the values coming from the final disposition of the carry

Based on the inputs given the outcome of operation is performed. As we know that the BK adder performs and executes the operation in parallel. The obtained output will be segmented into smaller pieces. There are different topologies used in BK adder, but the operator is associative. Based on topology the operation is performed.

By using the associative binary operations, the algorithms will be generalized. This generalized algorithms performs certain operations and computed with particular efficiency. Basically there are two procedures followed in the system, they are in first pass the prefix sum as are calculated from the processing unit. And in second pass known prefix values are computed from processing unit to get initial value. So along with that the system performs two read operations and one write operation. After this stages the entire operation is followed by registers to save the bits in effective way.

Here a methodology is employed to design BK adder. The experimental results mainly, depends on area, delay, and power consumption. The expense of additional area and remarkable will increase the power consumption. Compared with VLSI implementations, the BK adder will produce performance differently. The modern FPGAs employ the fast-carry chain process to get faster results. Our proposed multiplier and the existing multipliers in comparison complete one discipline multiplication in one of a kind numbers of clock cycles. Consequently, it is useful to apply electricity according to one multiplication as a performance measure for assessment and it

gives identical weight to each electricity and computational delay.

IV. RESULTS

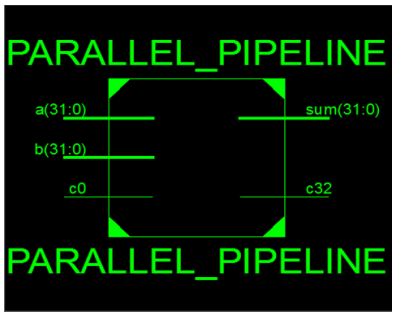

Fig. 2: RTL SCHEMATIC

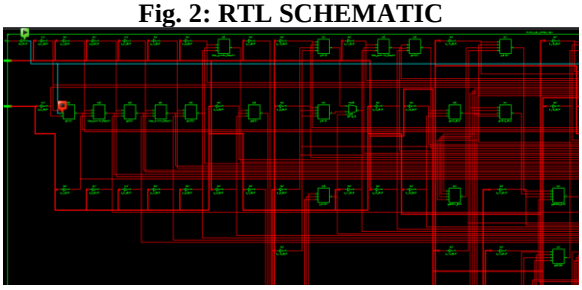

Fig. 3: TECHNOLOGY SCHEMATIC

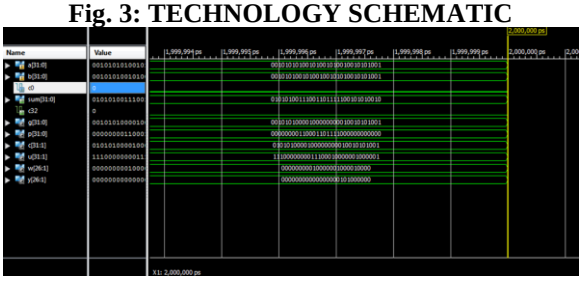

Fig. 4: OUTPUT

V. CONCLUSION

This paper is on the right track to formalize the process of designing the neural for designing Brent kung adder. The neural network Brent Kung adder functions correctly with different radices. It is very simple and unified. The hardware implementations are very simple and straightforward. The results demonstrate that it is possible to employ a systematic approach in designing neural networks for digital systems and that large-scale neural networks are capable of yielding high-quality solutions to complex problems. Hence the proposed system gives effective results compared to conventional one.

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