Design of a Multilevel Inverter with reduced number of carriers for PWM

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Abstract

In this paper a new topology with a reversing voltage component is proposed which will improve the multilevel performance by compensating the disadvantages of increased number of components, complex pulse width modulation control method and voltage balancing problem. This topology requires fewer components compared to existing inverter topologies (particularly in higher levels) and requires fewer carrier signals and gate drives. Therefore the overall cost and complexity are greatly reduced particularly for higher output voltage levels. This paper describes the general multilevel inverter schematic and modified circuit having only seven switches for seven- level multilevel inverter using reverse voltage topology. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. The simulation of a modified seven level multilevel inverter using reverse voltage topology is also presented here.

Keywords- *Multi-level inverter, Power electronics, Reverse voltage topology, SPWM*

Introduction

MLI's are used for high power and high voltage applications. MLI's have unique structure which makes it possible to reach high voltages with less harmonic content. Inverter is a device which converts dc power to ac power. Two level inverters require high switching frequency and disadvantages are less efficiency, high cost and high switching losses. Various PWM strategies are required to get high quality output which leads to high switching losses. MLI's are introduced to overcome these problems. MLI is able to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference. The advantages of MLI are improvement in staircase waveform quality, less input current distortion, lower electromagnetic interference. MLI's are used in drives, PV systems and automotive applications. The harmonic content of the output voltage waveform decreases as the number of output voltage increases.

MLI's are mainly classified as cascaded MLI, diode clamped MLI, flying capacitor MLI. The control method of cascaded H- bridge MLI because it doesn't have any clamping diode and flying capacitor. Cascaded MLI reaches higher reliability and this is used for large automotive electric drives. The main disadvantage is the increase in number of power switches that normally contributes to the complexity in con- trolling power switches. Many methods have been developed to decrease the number of switches. Modulation strategies applied to MLI's are selective harmonics elimination, carrier based PWM, space vector modulation, and fundamental frequency modulation. The PWM control is the most efficient method of controlling output voltage within the inverters. The carrier based PWM schemes used for MLI's is much more efficient, realized by the intersection of modulating signal with triangular carrier waveform. This paper is based on seven level inverter with reverse voltage topology which requires less number of switches than conventional topologies. This paper aims at generation of carrier based PWM scheme using PD method and can control output voltage and frequency and reduce the harmonic components in load currents. Here PD SPWM use ((n-1)/2) carriers to drive the inverter. In PD, all the carrier waveforms are in phase.

Multilevel Inverter Using Reverse Voltage Topology

Conventional cascaded MLI's require large number of switches and the power semiconductor switches are combined to produce an output in positive and negative polarity. In the new topology, there is no need to utilize all the switches in high frequency. This topology separates output voltage into level generation and polarity generation parts. Level generation part generates levels in positive polarity and polarity generation part generates the polarity of the output voltage. Level generation part needs high frequency switches and polarity generation part requires low frequency switches operating at line frequency.

Fig. 1 shows schematic diagram of a single phase seven- level reverse voltage topology. This MLI's can be increased to higher voltage levels by increasing middle section. This topology requires less switches and it can be applied to three phase application. The PD SPWM for proposed topology needs only half the number of conventional carriers for SPWM. PD SPWM for seven level conventional inverters requires six carriers, but in the proposed system only three carriers are need- ed.

MLI control with less number of carriers is the main ad- vantage in this topology. Separate dc sources are needed for this topology. The proposed MLI has better efficiency than conventional MLI.

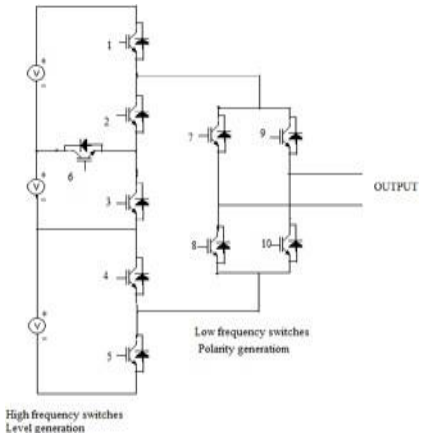

Figure 1 General single phase multilevel inverter (using reverse voltage topology) circuit

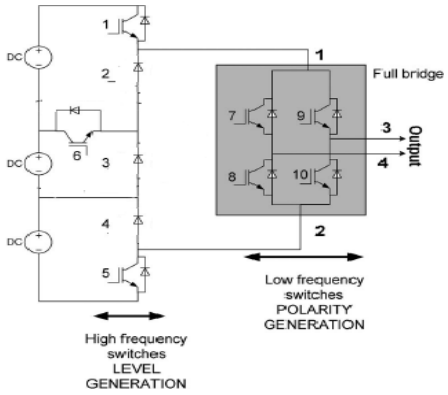

Figure 2 Proposed circuit using RV topology

In seven level inverters, ten switches and three dc sources are used. The left portion of the circuit in Fig. 1 generates the required output levels and the right portion of the circuit generates the polarity of the output voltage. The right portion of the circuit is called polarity generation part; it reverses the output of the level generation part, when the voltage polarity requires to be changed for negative polarity. MLI control is implemented using reduced number of carriers, which is a great achievement. Proposed topology does not need fast switches for the polarity generation part. The proposed MLI has better efficiency. The switching modes are selected such that to reduce the switching transitions for avoiding the un- wanted voltage levels. This will minimize the switching power dissipation. There are six possible switching patterns to control the multilevel inverter (see Table 1). The sequence of switches (2-3-4), (2-3-5), (2-6-5) and (1-5) are used for levels 0, 1, 2 and 3 respectively. The output voltage is the sum of volt- age sources, which are included in the current path.

TABLE 1 SWITCHING MODES

LEVEL / MODE	0	Vdc	2Vdc	3Vdc
1	2,3,4	2,3,5	1,4	1,5
2		2,4,6	2,6,5	

Proposed Circuit Using Reverse Voltage Topology

Reduced number of switches leads to reduced cost and complexity. This also leads to reduced losses and in- creased efficiency. This circuit requires only seven switches. Here high frequency switches 2, 3 and 4 in the general single phase multilevel inverter shown in Fig. 1 are replaced by diodes 2, 3 and 4. Fig. 2 shows the proposed circuit using re- verse voltage topology.

Modes of Operation

Fig. 3 shows the level 0 = 0 V_{dc} of seven level inverter. Here the diodes (2, 3, 4) are conducting to develop zero voltage. These switches are driven by PD-SPWM.

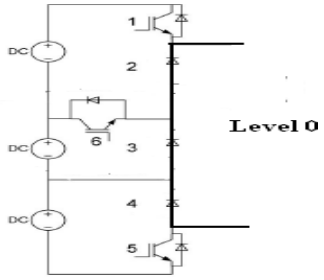

Figure 3. Level 0 = 0 V_{dc}

Fig. 4 shows the level 1 = V_{dc} of seven level inverter. Here the switch 5 and diodes (2, 3) are conducting to generate V_{dc}. Here one DC source is included.

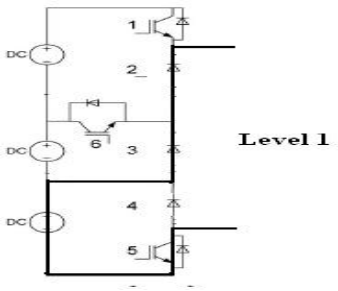

Figure 4. Level 1 = Vdc

Fig. 5 shows the level 2 = 2 Vdc of seven level inverter. Here the switches (6, 5) and diode 2 are conducting to generate 2 Vdc. Here two DC sources are included.

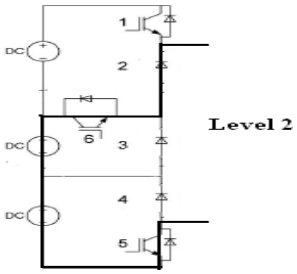

Figure 5. Level 2 = 2Vdc

Fig. 6 shows the level 3 = 3 Vdc of seven level inverter. Here the switches (1, 5) are conducting to generate 3 Vdc. Here three DC sources are included.

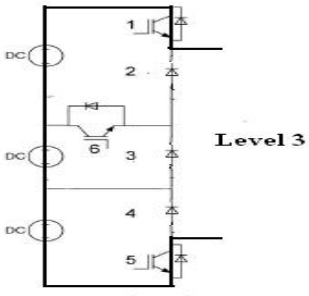

Figure 6. Level 3 = 3 Vdc

Control Strategy

The carrier based PWM technique fulfills the on and off states of the switches by comparing a modulating signal V_A (desired AC output voltage and a triangular waveform V_C (carrier signal). The modulating signal V_A is a sinusoidal signal at frequency F_C and amplitude V_A and the triangular signal V_C is at frequency F_C and amplitude V_C. This is the SPWM method. The modulation index is defined as $m_a = V_C/V_A$ and the normalized carrier frequency is $m_f = F_C/F_A$. PWM has the following advantages.

1. The entire control circuit is digital, digital control lines reduce the susceptibility to interference and also motors may be able to operate at lower speeds.
2. The output voltage control can be obtained without any additional components.
3. Lower order harmonics can be reduced along with its output voltage control.

In this topology, PD-SPWM is adopted for its simplicity and the carriers are in phase with each other. Here PD-SPWM is used for driving the high frequency switches and low frequency polarity generation part drive signals are generated with the line frequency (50Hz) and they only changes at zero- voltage crossings. For a conventional cascaded MLI, (n-1) tri- angle waveforms are used. In the proposed topology, a phase modulation signal is compared with (n-1)/2 triangle wave- forms for an n-level inverter.

One of the main advantages of this topology is that it re- quires less high frequency switches and the reliability of the system is indirectly proportional to the number of its components. As the number of high frequency switches is decreased, the reliability of the converter is increased. Hence the reliability is highly improved in this topology. Also high frequency switches are expensive and easily damaged. It can clearly be mentioned that the number of components of this topology is lower than that of other topologies and it will decrease tremendously with higher voltage levels. Switches in the full bridge converter are switched at line frequency.

Simulation Results

Simulation of proposed MLI is performed using MATLAB. The output waveforms of proposed multilevel inverter are given. All input DC sources are equal. MATLAB 7.10.0 (R2010a) is used for simulation part of the project.

Simulation of Proposed System

Simulation of the proposed topology of MLI is performed using MATLAB. Simulation results for the proposed system are given below. Modulation techniques are used in multilevel inverter to synthesis a controlled output voltage. There are various modulation techniques, of which phase disposition pulse width modulation is used here. Here phase disposition SPWM id used for driving the switches in the level generation part and switches in the polarity generation part are driven by the line frequency.

In this proposed topology, a phase modulation signal is compared with (n-1)/2 carriers for an n-level inverter and all the carriers are in phase. Since this converter works only in positive polarity, this topology requires half of the conventional carriers for SPWM controller. Here DC power supplies are adjusted to 50V and switching frequency is 4KHz. Output voltage is 300 Vp-p. In this proposed topology, a phase modulation signal is compared with (n-1)/2 carriers for an n-level inverter and all the carriers are in phase. The wave- form of proposed MLI with an inductive load is shown in Fig. 7.

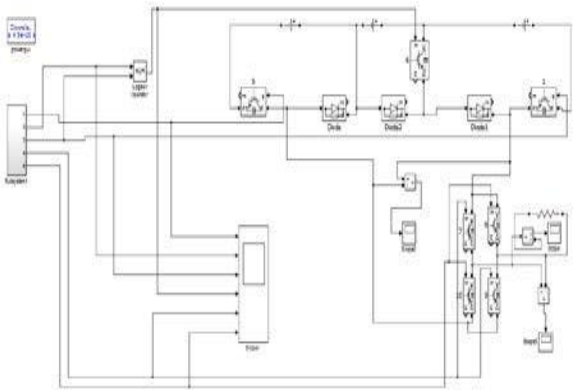

Figure 7. Simulation diagram of proposed system

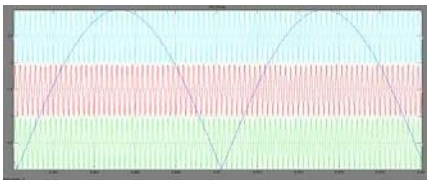

Figure 8. SPWM carrier and modulator

The proposed seven-level inverter consists of seven switches and three diodes and three DC sources. Subsystem consists of PWM generation. Here three carriers are compared with control signal. Levels generated are fed to polarity generation part; as a result seven levels are obtained. Output voltage is 300Vp-p.

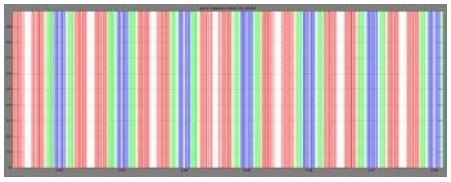

Figure 9. Gate signals for SPWM

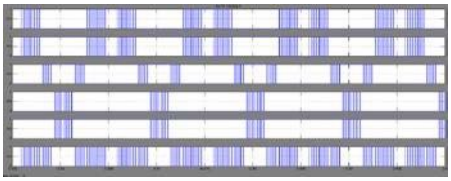

Figure 10. Complete gate signals for seven-level generation

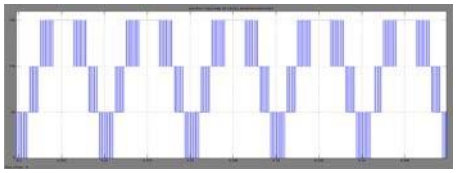

Figure 11. Output voltage of level generation part

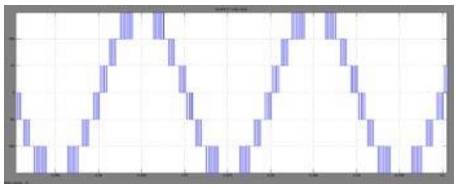

Figure 12. Output voltage of polarity generation part

Conclusion

MLI's have been used in many industrial applications like HVDC, FACTS, EV, PV systems, UPS, and industrial drive applications. In the proposed topology, switching operations are separated into high and low frequency parts. Instead of using cascaded inverter topology, proposed topology is better for all these applications because it has less control complexities, cost is also less and gives less % THD. Thus proposed topology is preferred than conventional cascaded inverter.

The PD-SPWM control method is used to drive the inverter. The PWM for this topology has fewer complexities since it only generates positive carriers for PWM control. This topology can effectively work as a multilevel inverter with a reduced number of carriers for PWM.

References

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