# Verge Logic Campaigns Comprising Of Sub Threshold CMOS Circuits

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***ABSTARCT:***

*A threshold-logic gate device consisting of sub threshold MOSFET circuits is proposed. The gate device performs threshold-logic operation, using the technique of current-mode addition and subtraction. Sample digital subsystems, i.e., adders and morphological operation cells based on threshold logic, are designed using the gate devices, and their operations are confirmed by computer simulation. The device has a simple structure and operates at low power dissipation, so it is suitable for constructing cell-based, parallel processing LSIs such as cellular-automaton and neural-network LSIs*

## INTRODUCTION:

The demand for low power electronics is rising day by day. In this era of hand held devices long battery life is a very important criterion for electronics industries. Everyone wants long battery life for their device. This all started from the Moore's Law. In 1965, Gordon Moore observed that the number of transistors that can be placed on a single IC (Integrated Circuit) of the same area has been doubling every two years [1]. It affected the semiconductor industry positively. Transistors shipped per year have increased exponentially as the average price per transistor has dropped off exponentially with the minimum feature size. An additional benefit of this scaling is the increased performance of circuits. From there The Integrated Circuits (ICs) world is accustomed till this point to following Moore's Law. But unexpectedly process scaling has a number of problems which blocks to move on exponentially. Some of them are

- Increased power dissipation
- Increased complexity etc.

Main concern which hampers the further scaling of transistors is the issue of power dissipation. A chip consist of many energy storage elements, mainly capacitors, some that are required for computation (MOSFET device capacitances) and some that are a hindrance to circuit operation (parasitic capacitances). These capacitors are continually charged and discharged through resistive elements during circuit operation, resulting in energy dissipation in the form of heat. The amount of heat dissipated puts a restriction on the computational performance of the circuit. While shrinking of devices has reduced the amount of parasitic capacitance and this alleviates power dissipation problems. But the number of devices (dissipating power somewhat less) accommodated has been increased due to process scaling which results in more power dissipation as compared to previous one. As the more number of transistors are placed on a single chip, the sub- threshold leakage current becomes dominant factor of total power dissipation. Sub-threshold leakage current occurs when transistor is off. So the leakage current dissipates power, even when it is not doing any useful computations, in the form of heat. The MOS-FET threshold voltage VT decreases with increase in the device junction temperature caused by this heat dissipation. The sub-threshold leakage currents are exponentially dependent on VT, increasing with decrease in VT. Thus increased on-chip temperatures cause more power dissipation due to increased leakage currents and increased dissipation of heat. Another problem with aggravated on chip temperature is that they can result in reduced operating life spans for the chip

**SUB-THRESHOLD LOGIC** As seen above the sub threshold current is present in our circuit, but is of no use. So let us use these subthreshold current for operation of our circuit. The idea of using sub-threshold current for circuit is known as subthreshold logic. Here the VDD of the circuit is set at a value lower than or equal to the threshold voltage of that particular process technology, i.e. VDD ≤ VT. Figure 2.1 shows the dependence of drain current (ID) on applied Gate to Source voltage (VGS). This can be seen that below threshold voltage the current through the transistor is exponential in nature. The circuit will thus operate with only sub-threshold leakage currents, since the transistors in the circuit will never be in the linear or saturation region. This approach not only results in very low power consumption but it also utilizes leakage currents for computation.

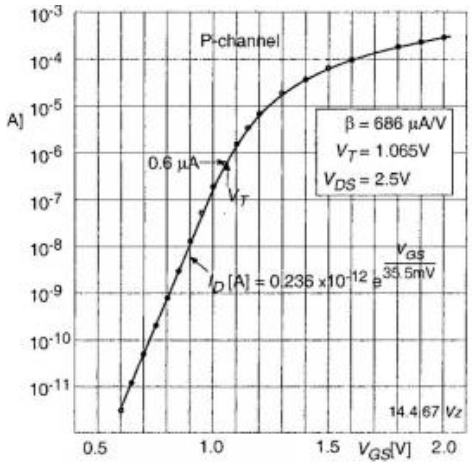



Fig. 2.1: ID versus VGS plot, for 0.18µm process with VDD = 1.8V

## LITERATURE SURVEY

**1.IN "S. Bobba and I. N. Hajj, "Current-mode threshold right judgment gates," in Proc. IEEE ICCD, Sep. 2000, pp. 235–240"** In this paper, we present low-strength and excessive-ordinary overall performance commonplace revel in gates known as the modern-day-day-mode threshold good judgment (CMTL) gates. Low-energy dissipation is completed by means of limiting the voltage swing at the interconnects and the inner nodes of the CMTL gates. High-overall performance is completed via manner of the use of using transistor configurations that revel in a small distinction in cutting-edge and set the differential outputs to the proper values. The attention of NAND, NOR, AND, OR common revel in gates and unique not unusual experience features the usage of the CMTL gates is provided. We furthermore gift numerous implementations of CMTL gates and describe the relative benefits and boundaries of those implementations. SPICE simulation, results for a 1.5 V 0.18 u CMOS technology are also supplied for the precise circuit configurations defined in the paper

The format of circuits using extraordinary nicely judgment families consequences in circuits with wonderful commonplace overall performance and strength dissipation. A description of the best of a kind commonplace experience households and their strengths/ weaknesses can be placed in [l]. The capability of a common experience gate inside the non-clocked good judgment households which embody static CMOS, differential cascode voltage transfer commonplace experience (DCVS) [2], skip-gate good judgment, and clocked not unusual experience households which embody unmarried-rail domino, dual-rail domino, latched domino systems [3-

fifty one and clocked skip-gate desirable judgment is primarily based totally on the the usage of transistor as an ON/ OFF switch. For first-rate enter venture, a few transistors flip ON (or OFF) and it connects (or disconnects) the output node of the not unusual revel in gate to one of the supply rails (Vdd/ Gnd) via the zero,N (or OFF) transistors. In order to honestly flip ON or flip OFF a transistor, the voltage swing at the gate input of the transistor should be from Gnd to Vdd or from Vdd to Gnd. Since the input to a few correct judgment gate is also the output of a few different not unusual enjoy gate, it method that the output nodes of properly judgment gates want to moreover make full voltage swings. The energy dissipated through a circuit is proportional to the square of the supply voltage. In order to the reduce the electricity dissipation, the supply voltage can be decreased which results in a decrease voltage swing. Lower supply voltage moreover outcomes in reduced power strength and average preferred normal overall performance degradation for the common feel gates. An change technique is the format of suitable judgment gates wherein the transistors are not required to actually flip-ON/ turnOFF. In [6], the nice judgment gates are operated inside the subthreshold vicinity and the transistors aren't surely have come to be ON. But the slow operating pace of those not unusual feel gates limits their software to low pace circuits. In this paper, we use low swing enter voltages and impose the format constraint that a transistor can't be grew to become OFF. The functional dependence of the ON-transistor homes (transconductance) on the enter voltage desires for use in the layout of those common enjoy gates. This requires a excessive-benefit diploma that could sense the difference inside the transconductance or the present day pushed thru the transistors to set the output to the correct values. This can be acquired with the useful resource of way of the use of using the latched domino shape. The latched domino systems [three-fifty one can offer immoderate-regular commonplace universal overall performance through using the latch shape as a senseamplifier. The versions the various winning artwork and the proposed paintings are one or greater of the following: Most latched domino circuits are used with differential nMOS tree wherein only considered one in every of output nodes is pulled down thru the differential nMOS tree. In the proposed artwork, the good judgment circuitry isn't always differential and each units of transistors are continuously ON. In latched domino circuits, the nMOS not unusual experience circuit and the latch are connected to the output nodes in parallel. This manner that there are a couple of paths to charge or discharge the output nodes. In our proposed artwork, the commonplace enjoy community seems at the direction from Vdd to the output node. By

modulating the contemporary that prices the output node, we set the output to the proper price. This will boom the sensitivity of the commonplace enjoy gate and offers it with the capability to revel in small distinction in currents. In latched domino circuits, the first-class judgment network includes nMOS transistors with complete enter swings. In the proposed art work, we use PMOS transistors inside the proper judgment community with small voltage swings.

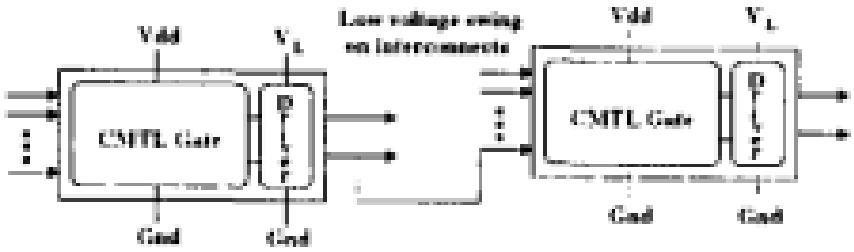



Figure : Circuit with CMTL gates

**2.In "T. Ogawa, T. Hirose, T. Asai, and Y. Amemiya, "Threshold-logic devices consisting of subthreshold CMOS circuits," *IEICE Trans. Fundam. Electron., Commun. Comput. Sci.*, vol. E92-A, no. 2, pp. 436–442, 2009."** A threshold-common feel gate device which include subthreshold MOSFET circuits is proposed. The gate tool performs threshold-commonplace revel in operation, the use of the method of current-day-day-mode addition and subtraction. Sample virtual subsystems, i.E., adders and morphological operation cells based absolutely totally on threshold commonplace feel, are designed the usage of the gate gadgets, and their operations are confirmed thru computer simulation. The device has a easy form and operates at low electricity dissipation, so it's miles suitable for constructing cell-based totally, parallel processing LSIs inclusive of cell-automaton and neural-community LSIs

**3.IN "W. Prost et al., "Manufacturability and sturdy layout of nanoelectronic not unusual feel circuits based totally on resonant tunnelling diodes," Int. J. Circuit Theory Appl., vol. 28, no. 6, pp. 537–552, Nov./Dec. 2000."**The manufacturability of precise judgment circuits based totally mostly on quantum tunnelling devices, specifically double-barrier resonant tunnelling diodes (RTD), is studied in element. The homogeneity and reproducibility of III/V mesa technology-primarily based devices is experimentally evaluated and interpreted using multiple I–V feature simulations. The experimental sensitivity of the RTD I–V parameters on

nicely and barrier thickness is in evaluation with more than one I–Vsimulations. With shrinking minimum function period the fluctuations in the top contemporary may be immediately attributed to an RTD vicinity model because of the growing impact of lithography and etching on lateral dimensions. These outcomes show that the III/V era fulfils the necessities for a massive scale integration of RTD devices. A nanoelectronic circuit form based totally totally totally on an advanced MOBILE threshold good judgment gate is provided. Detailed SPICE simulations the usage of the experimental facts show that clock and deliver voltage fluctuations are tolerated as plenty as ± 0.1 V at a supply voltage of zero.7 V. Very strong nearby height voltage variations of 15 in line with cent in opposite suggestions might be important to have a vital impact immediately to the circuit capability. Smaller deviations satisfactory have an impact on the timing with out degrading the reliability of the circuit. Consequently, the format of a robust energy deliver and clocking scheme is extra essential for the general circuit normal average performance than the small relative deviations of the RTD pinnacle voltage

**4.In "S. Muroga, Threshold Logic and Its Applications. New York, NY, USA: Wiley, 1971"**As an technique to clarifying the primary houses of threshold commonplace experience, the completely monotonic feature is investigated. Its trying out approach, purposeful shape, and so forth., are noted through the usage of a present day concept, mutual monotonicity.

**MAJORITY-BLACK CIRCUIT CONSISTING OF THRESHOLD LOGIC GATES**

As a promising software program program of our thrshold commonplace experience gate we are designed celular automation cells that carry out morphological operations for image processing. The following suggests a part of the cease end result, taking the majrity black operation for example. The majority black operation is a morhological photo processing for binary pics. It is beneficial for filling sma hoes and eliminating small projections in gadgets and,therefore may be used for nois removal . The majority bck operation is as follows processing for three*3 pixels winws are black if five or extra pixels within the three×3window are black; in any other case set the center pixel to white In image processing, the majorityblack operation is completed in all pixels on a picture synchronously with a clock.The mobile characteristic of majority black operation may be completed the usage of 9 enter majority gate circuit showed in

11111111 + 00000001=100000000

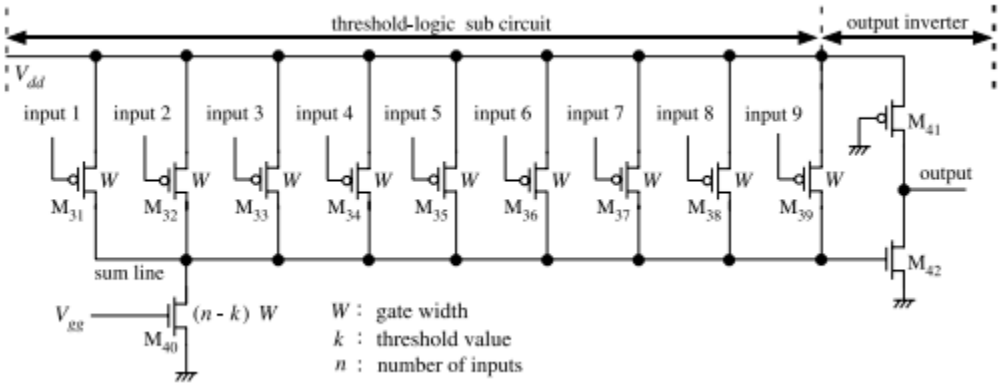
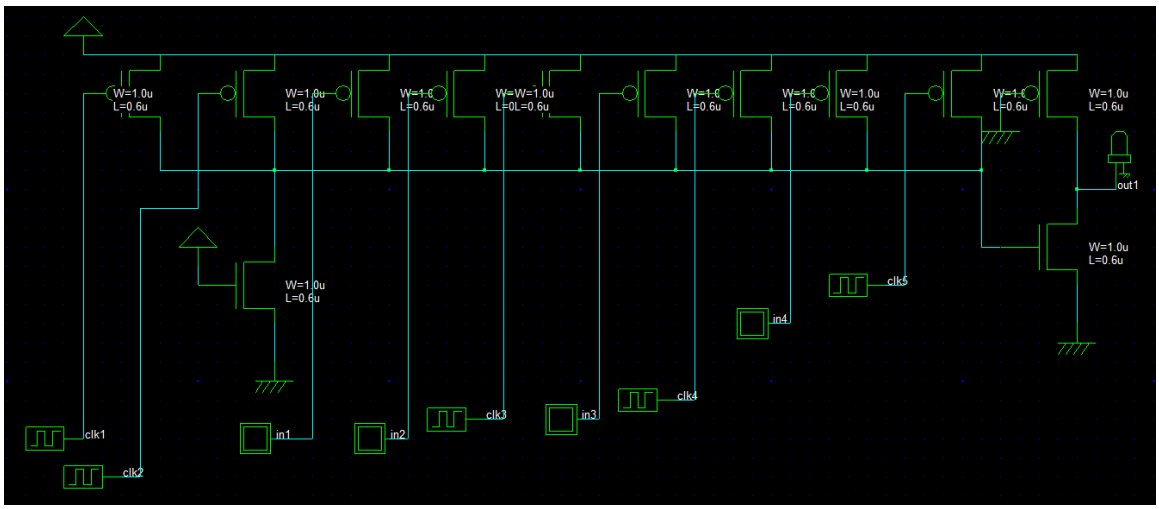
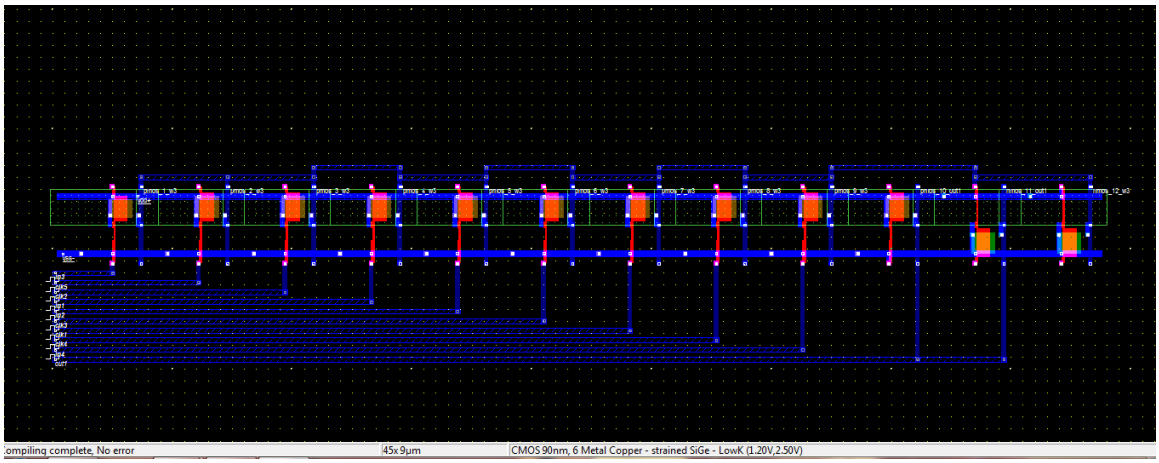


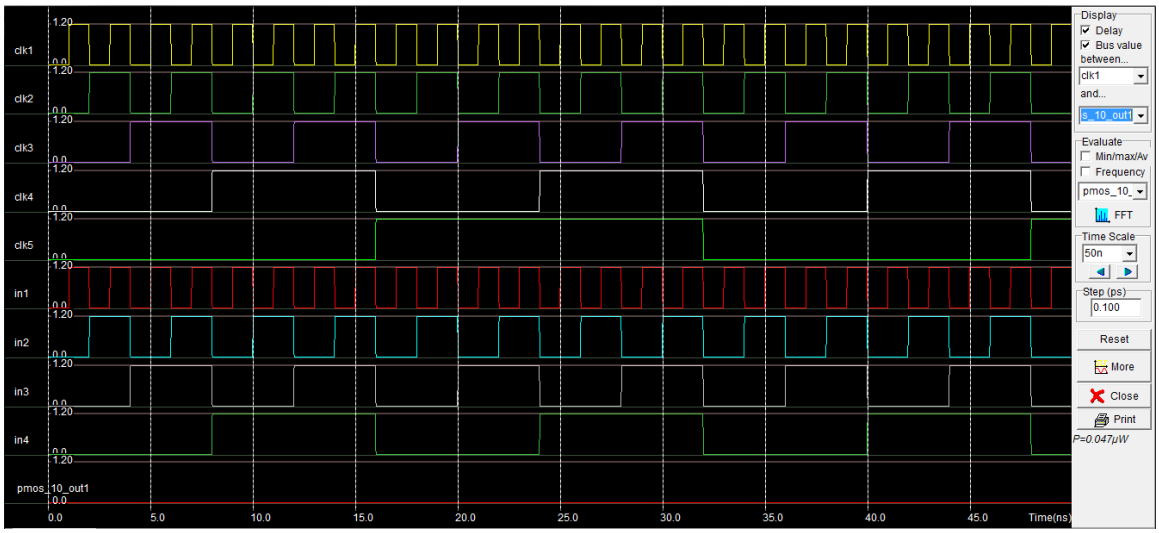

**Fig: Majority block circuit using threshold logic gate**

fig every enter corresponds to the dominion of every pixel in the 3*3 window we outline that the enter is 1voltage if the pixel s black and the input is 0 if the pixel is white the output of the corresponds to the subsequent u . S . A . Is black for a 1 output and white for zero output. If the range f 1 input s for M31-M39 is better than the edge te internet modern-day injected to the sum line is terrible

**SIMULATION RESULTS**






## CONCLUSION:

An analytical technique has been proposed to find out short the transistor size in the sensor factor of a modern mode implementation that guarantees very low gate put off (very close to the minimum), unbiased of the modern-day-day mode technique used to enforce the edge genuine judgment characteristic. A new cutting-edge mode implementation approach have grow to be moreover proposed that outperforms present implementations every in gate cast off in addition to energy

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