

VLSI Design Of High Speed Dynamic Accuracy Configurable Multipliers By Using Compressor Technique

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Abstract— In this paper, we propose four 4:2 compressors, which have the flexibility of switching between the exact and approximate operating modes. Multiplication is basic function in arithmetic operations. Multiplication based operations such as multiply and Accumulate unit (MAC), convolution, Fast Fourier Transform (FFT), filtering are widely used in signal processing applications. As, multiplication dominates the execution time of DSP systems, there is need to develop high speed multipliers. In the approximate mode, these dual-quality compressors provide higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors has its own level of accuracy in the approximate mode as well as different delays and power dissipations in the approximate and exact modes. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of these compressors in a 8-bit Dadda multiplier are evaluated using VerilogHDL and simulated and synthesized using XILINX ISE design suit. Comparing their parameters with those of the existing Wallace tree multiplier designed using 4:2 and 5:2 compressors. The results of comparison indicate the lower delay and power consumption in the approximate mode.

Index Terms— 4:2 compressors, accuracy, approximate computing, configurable, delay, power.

I. INTRODUCTION

Motivated by the limited research on approximate multipliers, compared with the extensive research on approximate adders, and explicitly the lack of approximate techniques targeting the partial product generation, we introduce the partial product perforation method for creating approximate multipliers. We omit the generation of some partial products, thus reducing the number of partial products that have to be accumulated; we decrease the area, power, and depth of the accumulation tree. By reducing the quality (accuracy), the delay and/or power consumption of the unit may be reduced. In addition, some digital systems, such as general purpose processors, may be utilized for both approximate and exact computation modes [4]. An approach for achieving this feature is to use an approximate unit along with a corresponding correction unit. The correction unit, however, increases the delay, power, and area overhead of the circuit. Also, the error Correction procedure may require more than one clock cycle, which could, in turn, slow down the processing further.

The most commonly used techniques for the generation of approximate arithmetic circuits are truncation, voltage over scaling (VOS) and simplification of logic. Extensive research has been conducted on approximate address providing significant gains in terms of area and power while exposing small error. To meet the power and speed specifications, a variety of strategies at totally different style abstraction levels are suggested. Approximate computing approaches are supported achieving

the target specifications at the value of reducing the computation accuracy [4]. The approach is also used for applications wherever there's not a singular answer and/or a group of answers close to the correct result are often thought-about acceptable [5]. These applications include multimedia system process, machine learning, signal process, and different error resilient computations. Approximate arithmetic units are primarily based on the simplification of the arithmetic units circuits [6]. There are several previous works that specialize in approximate multipliers which give higher speeds and Lower power consumptions at the value of lower accuracies. Almost, all of the projected approximate multipliers are primarily based on having a set level of accuracy throughout the runtime. The runtime accuracy reconfigurability, however, is taken into account as a helpful feature for providing totally different levels of quality of service throughout the system operation [6]–[8]. Here, by reducing the standard (accuracy), the delay and/or power consumption of the unit is also reduced. Additionally, some digital systems, like general purpose processors, are also utilized for each approximate and precise (Exact) computation modes [4].

An approach for achieving this feature is to use an approximate unit alongside a corresponding correction unit. The correction unit, however, will increase the delay, power, and space overhead of the circuit. Also, the error correction procedure could need more than one clock cycle (see [9]), that might, in turn, slow down the process additional. In this paper, we have a tendency to propose four dual-quality reconfigurable approximate 4:2 compressors, which give the flexibility of switching between the precise (Exact) and approximate operative modes during the runtime. The compressors are also utilized within the architectures of dynamic quality

configurable parallel multipliers.

The fundamental structures of the projected compressors consist of 2 components of approximate and supplementary. In the approximate mode, solely the approximate half is active whereas in the actual operative mode, the supplementary half alongside some parts of the approximate half is invoked.

The rest of this paper is organized as follows. In Section II, some prior works on the approximate multipliers are reviewed. Existing compressor are explained in Section III. Implementation of proposed compressors in 8-bit dadda multipliers is explained in section IV. Results and discussions are explained in chapter VI. Finally, this paper is concluded in Section VII.

II. LITERATURE SURVEY

In [1], by modifying the Karnaugh map of a two \times two multiplier, AN approximate 2×2 multiplier with a simpler structure has been projected. An inaccurate multiplier style strategy supported redesigning the multiplier into 2 multiplication and non-multiplication parts was introduced. The multiplication half was constructed supported the traditional multipliers whereas the non-multiplication half was enforced in AN approximate structure with such as worth of error. It ought to be noted that each of the approaches given in [1] and [12] suffer from high relative errors.

In [10], a static section methodology (SSM) is given, that performs the multiplication operation on an mbit section ranging from the leading one little bit of the input operands wherever m is adequate to or bigger than $n/2$. Hence, an $m \times m$ multiplier consumes a lot of less energy than other multiplier. Also, a dynamic vary un biased multiplier (DRUM) multiplier, that selects an mbit section, starting from the leading one little bit of the

input operands, and sets the least important little bit of the truncated values to “1,” has been proposed in [11]. During this structure, the truncated values are multiplied and shifted to the left to come up with the ultimate output. Although, by exploiting smaller values for m, the structure of [11] provides higher accuracy styles than those of [10], its approach needs utilizing additional complicated electronic equipment.

In [15], a high accuracy approximate 4×4 Wallace tree multiplier was projected. This multiplier utilized a 4:2 approximate counter resulting in delay and power reductions of the partial product stage of the 4×4 Wallace tree. During this paper, the proposed little multiplier was went to type larger multipliers. Due to the array structure of this approximate multiplier, its delay was giant. Additionally, an EDC unit was urged to be used at the output of the approximate four × four Wallace tree. The unit generated the precise output within the case of the exact operational mode. In [16], by proposing an approximate adder with a little carry propagation delay, the partial product reduction stage was sped up. During this paper, an OR-gate-based error reduction unit was additionally projected. In [17], a rounding based approximate multipliers (ROBA) has been projected that round the input operands into the closest exponent of 2. This way the multiplication operation became less complicated. It ought to be noticed that the error recovery unit (those in [1], [12], [15], and [16]) will increase the ability consumption and delay of the multiplier.

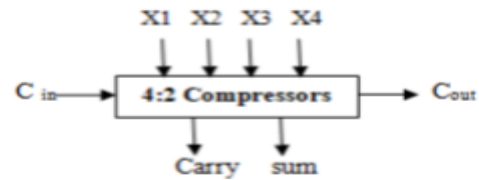


Fig.1. Block diagram of 4:2 compressors.

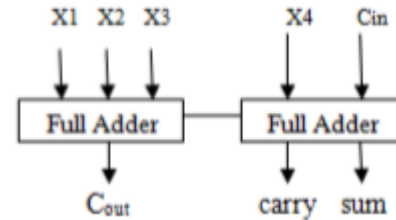


Figure 2: Structure of the conventional 4:2 compressor.

This means that accuracy configurable multipliers would have large delay and power overheads. In this paper, we propose compressors, which have the ability of switching between the approximate and exact modes with very small delay and power overheads.

III.EXISTING SYSTEM

First, some background on the exact 4:2 compressor is presented. This type of compressor, shown schematically in Fig. 1, has four inputs (x1–x4) along with an input carry (Cin), and two outputs (sum and carry) along with an output Cout. The internal structure of an exact 4:2 compressor is composed of two serially connected full adders, as shown in Fig. 2. In this structure, the weights of all the inputs and the sum output are the same whereas the weights of the carry and Cout outputs are one binary bit position higher. The outputs sum, carry, and Cout are obtained from

$$\text{sum} = x1 \oplus x2 \oplus x3 \oplus x4 \oplus \text{Cin} \quad (1)$$

$$\text{carry} = (x1 \oplus x2 \oplus x3 \oplus x4) \text{Cin} + (x1 \oplus x2 \oplus x3 \oplus x4)'x4 \quad (2)$$

$$\text{Cout} = (x1 \oplus x2)x3 + (x1 \oplus x2)'x1. \quad (3)$$

The compressor 4:2 trees also has a regular

structure and sums the partial products as a binary tree does, using 4:2 compressors instead of CSAs.

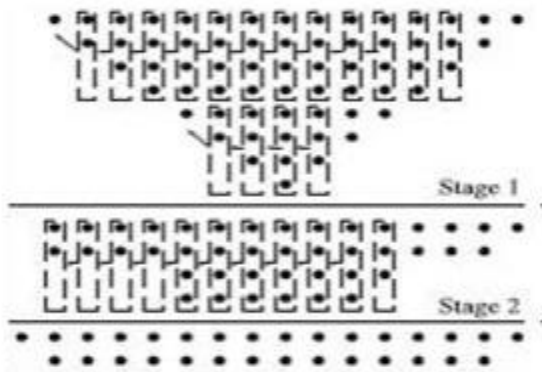


Figure 3. Dot diagram for a multiplier using exact 4:2 compressor

IV .PROPOSED 4:2COMPRESSORS

We present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked.

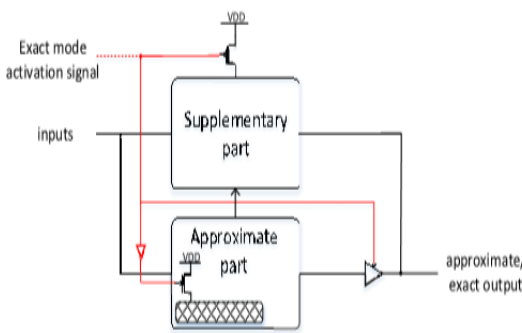


Figure 4: Block diagram of the proposed

approximate 4:2 compressors. The hatched box in the approximate part indicates the components, which are not shared between this and supplementary parts.

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors is shown in Fig. 4. The diagram consists of two main components of approximate and supplementary. During the approximate mode, solely the approximate half is exploited while the supplementary half is power gated. During the exact in operation mode, the supplementary and a few components of the approximate components are utilized. Within the planned structure, to reduce the facility consumption and space, most of the components of the approximate half also are used through out the exact in operation mode. we have a tendency to use the facility gating technique to turn OFF the unused elements of the approximate half. Also note that, as is clear from Fig.4, within the precise in operation mode, tri-state buffers are utilized to disconnect the outputs of the approximate half from the first outputs. During this style, the shift between the approximate and precise in operation modes is quick. Thus, it provides us with the chance of designing parallel multipliers that are capable of shift between completely different accuracy levels throughout the runtime. Next, we discuss the main points of our four DQ4:2C's

1) Structure 1 (DQ4:2C1):

For the approximate a part of the first projected DQ4:2C structure, as shown in Fig. 5(a), the approximate output carry (i.e., carry) is directly connected to the input x4 (carry = x4), and also, in an exceedingly similar approach, the approximate output add (i.e., sum) is directly connected to Fig. 5. (a) Approximate half and (b) overall structure of DQ4:2C2. Input x1 (sum = x1). Within the approximate a part of this structure, the output Cout is neglected. whereas the approximate a

part of this structure is significantly quick and low power, its error rate is large (62.5%).

The supplementary part of this structure is a definite 4:2 Compressors. the structure of the projected structure is shown in Fig. 5(b). within the actual operative mode, the delay of this structure is concerning identical as that of the precise 4:2 compressors.

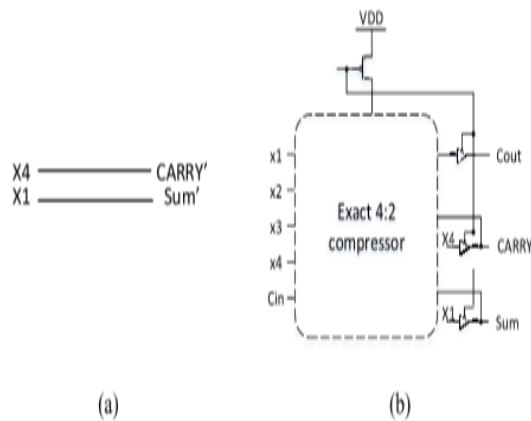


Figure 5: (a) Approximate part and (b) overall structure of DQ4:2C1

2) Structure 2 (DQ4:2C2):

Within the initial structure, while ignoring Cout simplified the interior structure of the reduction stage of the multiplication, its error was massive. Within the second structure, compared with the DQ4:2C1, the output Cout is generated by connecting it on to the input x3 within the approximate half. Fig. five shows the interior structure of the approximate half and also the overall structure of DQ4:2C2. While the error rate of this structure is that the same as that of DQ4:2C1, namely, 62.5%, its relative error is lower.

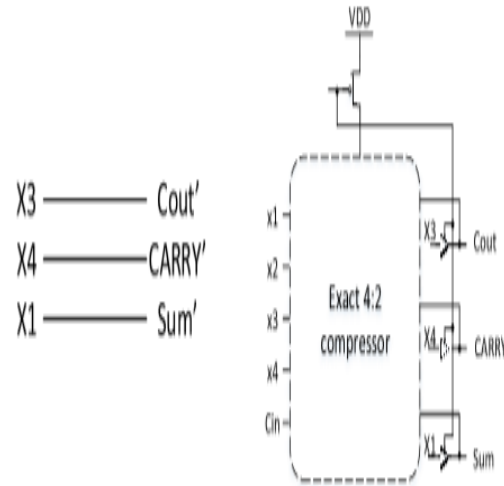


Figure 6: (a) Approximate part and (b) overall structure of DQ4:2C2.

3) Structure3 (DQ4:2C3):

The previous structures, in the approximate operative mode, had most power and delay reductions compared with those of the precise compressor. In some applications, however, a better accuracy could also be needed. Within the third structure, the accuracy of the approximate operating mode is improved by increasing the complexness of the approximate half whose internal structure is shown in Fig. 7(a). During this structure, the accuracy of output ads is inflated. The same as DQ4:2C1, the approximate part of this structure doesn't support output Cout. The error rate of this structure, however, is reduced to five hundredth. The overall structure of DQ4:2C3 is shown in Fig. 7(b) where the supplementary half is embedded in an exceedingly red broken line rectangle.

Note that during this structure, the utilized NAND gate of the approximate half (denoted by a blue line rectangle) is not used throughout the precise operative mode. Hence, during this operative mode, we propose disconnecting provide voltage of this gate by mistreatment the power gating.

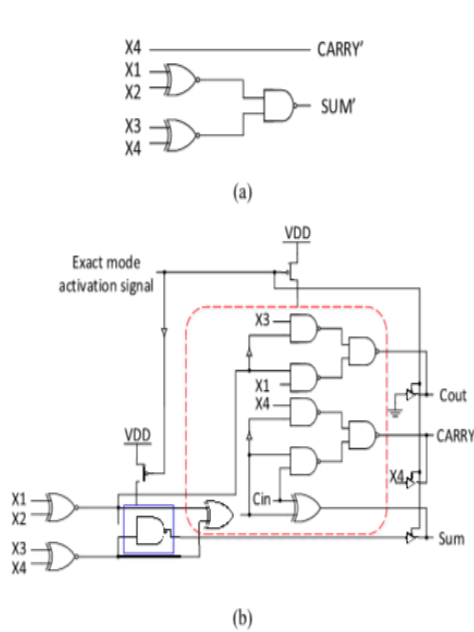


Figure 7: (a) Approximate part of DQ4:2C3 and (b) overall structure of DQ4:2C3

4) Structure4 (DQ4:2C4):

During this structure, we tend to improve the accuracy of the output carry compared there upon of DQ4:2C3 at the value of larger delay and power consumption wherever the error rate is reduced to 31.25%. The interior structure of the approximate half and therefore the overall structure of DQ4:2C4 are shown in Fig.8. The supplementary half is indicated by red dashed line rectangular whereas the gates of the approximate half, powered OFF throughout the precise Operational mode, are indicated by the blue line.

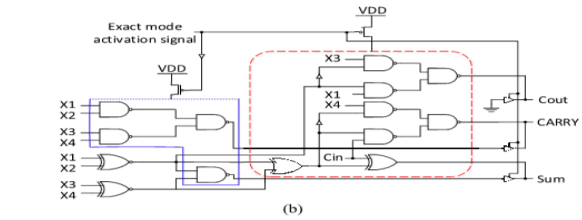
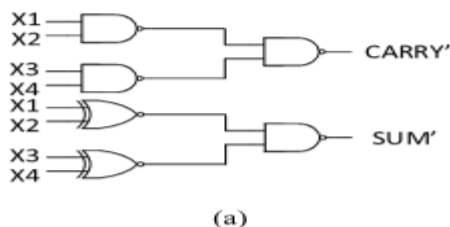


Figure 8: (a) Approximate part of DQ4:2C4 and (b) overall structure of DQ4:2C4

V.ACCURACY STUDY OF MULTIPLIER REALIZED BY THE PROPOSED COMPRESSORS

In this section we are going to implement the proposed dual quality 4:2 compressors on 8-bit dadda multiplier. And we will observe how these designs reduce the power, delay, area of the multiplier circuits. Fig 9. Shows the reduction circuitry of 8-bit dadda multiplier.

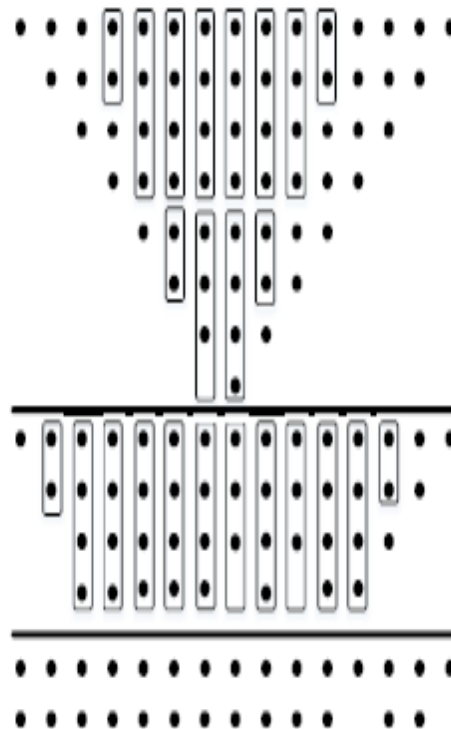


Fig.9. Reduction circuitry of an 8-bit daddamultiplier.

A proper combination of the proposed compressors may be utilized to achieve a better tradeoff between the accuracy and

design parameters. As an option, the use of both DQ4:2C1 and DQ4:2C4 for the LSB and MSB parts in the multiplication, respectively, is suggested here. The results for this multiplier are denoted by DQ4:2Cmixed. These multipliers are compared by the approximate Dadda multipliers implemented by two prior proposed approximate 4:2 compressors as well as the configurable multiplier. In addition, some state of-the-art approximate multiplier designs, which do not use approximate compressors, are considered. These multipliers include 32-bit unsigned ROBA (U-ROBA), SSM with a segment size 8 (SSM8), and DRUM with a segment size 6 (DRUM6). The general structure of the reduction circuitry in an 8-bit Dadda multiplier, which makes use of 4:2 compressors, is drawn in Fig.9.

V RESULTS AND DISCUSSION

In this section, the investigation, which is performed by utilizing proposed dual quality 4:2 compressors in the Dadda structure, the design parameters of the multipliers are compared with those of the exact Dadda multiplier, approximate Dadda multipliers realized using the two approximate 4:2 compressors proposed in [14], and the approximate multiplier presented in [15]. Also, XILINX ISE 14.4 design suite was used to synthesis and simulated the design. And the parameters of existing system were also taken as reference values in order to compare with the proposed design.

Next, the effectiveness of the proposed compressors in their exact operating mode utilized in the Dadda multiplier will be compared with that of the proposed approximate multiplier by [15] in the same mode. To extract the design parameters of the multipliers, we employed using XLINX ISE on Spartan 3E FPGA family.

Finally, all the studied approximate multipliers are compared based on different accuracy and design parameters.

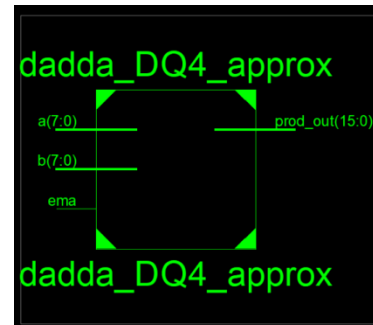


Fig .10 Top level block of DQ4 approximate.

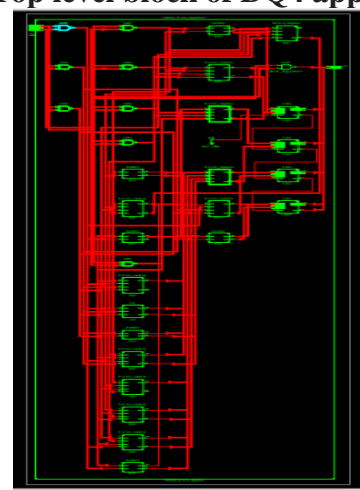


Fig 11.RTL schematic of proposed dual quality 4:2 compressors implemented on Dadda multiplier

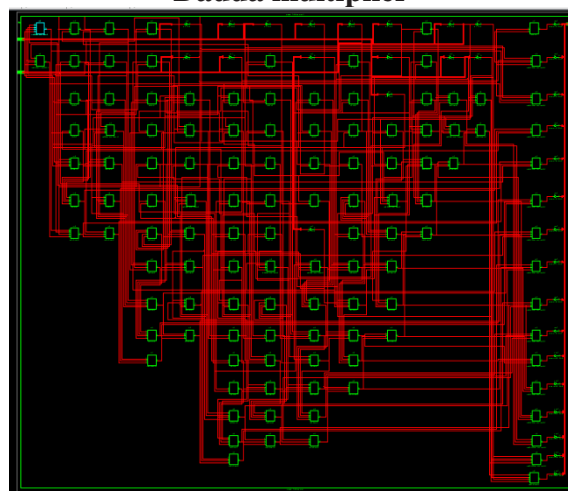


Fig 12. Technology schematic of proposed dual quality 4:2 compressors implemented on Dadda multiplier.

Device Utilization Summary (estimated values)				
Logic Utilization	Used	Available	Utilization	
Number of Slices		68	14751	0%
Number of 4 input LUTs		118	25514	0%
Number of bonded I/Os		32	261	12%

Fig 13. Design summary of proposed dual quality 4:2c4 Compressors.



Fig.14 Simulation result of proposed Approximate DQ4:2C4 compressor implemented in 8 bit dadda multiplier

VI. CONCLUSION

In this project, we have a tendency to propose four DQ4:2Cs that had the flexibility of change between the exact and approximate operating modes. Within the approximate mode, these compressors provided higher speeds and lower power consumptions at the cost of lower accuracy. Every of those compressors had its own level of accuracy within the approximate mode moreover as different delays and powers within the approximate and exact modes. The proposed compressors are

implemented on structure of a 8-bit Dadda multiplier, to estimate the performance of the proposed compressors. Our studies disclosed that for the 8-bit multiplication, the projected compressors have lower delay and power consumption within the approximate mode compared with those of existing compressors.

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