# Analysis of FinFET Architecture and Its Fabrication Mechanism

**Dr. R. Prakash Rao,**
*Associate Professor, ECE Department, Matrusri Engineering College, Saidabad, Hyderabad. India.*
*prakashiits@gmail.com*

## *Abstract*

*In view of difficulties of the planar MOSFET technology to get the acceptable gate control over the channel FinFET technology based on multiple gate devices is better technology option for further shrinking the size of the planar MOSFET [1]. For double gate SOI- MOSFET the gates control the channel created between source and drain terminal effectively. So the several short channel effects like DIBL, subthreshold swing, gate leakage current etc. without increasing the carrier concentration into the channel.*

*This paper mainly deals with detail description about the DG MOSFET structure and its particular type named as FinFET technology and its fabrication mechanism is also described. Below the 50nm technology FinFET has better controlling over the several short channel effects.*

*In section one the introduction is given, section two describe the Evaluation from previous technology, section three describe the DG MOSFET structure and its type, section four describe the FinFET technology, section five describe the fabrication mechanism of the FinFET technology and finally conclusions given in section six.*

***Keywords:*** *CMOS scaling, DG MOSFET, FinFET, Short Channel Effect, SOI Technology*

## 1. Introduction

When we shrinking further the size of the planar MOSFET technology several short channel effects are produced. So instead of planar MOSFET technology DG-MOSFETs technology based on multiple gates device have better controlling over the SCEs. Particularly the FinFET technology provides superior scalability of the DG-MOSFETs compare to the planar MOSFET. It provides better performance compare to the bulk Si-CMOS technology. Because of its compatibility with the recent CMOS technology FinFETs are seen to be strong candidate for replacing the bulk or planar Si-CMOS technology from 22nm node onwards. Many different ICs like digital logic, SRAM, DRAM, flash memory etc. have already been demonstrated. Due to their better controlling over subthreshold leakage current and current saturation FinFETs are advantages for the high gain analog applications and get better result in the RF applications [2].

Scaling planar CMOS to 10nm and below would be exceptionally difficult but not completely impossible, due to electrostatics, excessive leakages, mobility degradation, and many realistic fabrication issues. Particularly, control of leakage in a nano scale transistor would be critical to high performance chips such as microprocessors. Non-planar MOSFETs provide potential advantages in packing density, carrier transport, and device scalability [3].

## 2. Evaluation & Comparison of FinFET Technology

As devices shrinking further, the problems with the planar or bulk Si-CMOS technology are increasing. Several short channel effects like $V_T$ rolloff, drain induced barrier lowering (DIBL), increasing leakage currents such as subthreshold S/D leakage, gate induced drain leakage (GIDL), gate direct tunneling leakage, and hot carrier effects produced in the devices which degrading the use in industry. When power supply voltage $V_{dd}$ is reduced which helps to reduced power and hot carrier effects but the performance improvement is not good. Performance can be improved by lowering the $V_T$. Researcher are on search to find high-k gate dielectric so that a thicker physical oxide can be used help to reduce gate leakage and yet have adequate channel control, but this is not successful at the point of being usable. There are other problems with Si are band alignment, thermal instability problem etc. The thermal instability problem has led researchers to search for metal gate electrodes instead of polysilicon. But metal gates with suitable work functions have not been found to the point of being usable. In the absence of this, polysilicon continues to be used, whose work function

require that $V_T$ be set by high channel doping concentration which in turn leads to random dopant fluctuations (at small gate lengths) as well as increased impurity scattering and therefore reduced mobility [4]. The off-state leakage current and standby power are increasing with shorter channel-lengths since it is becoming more difficult to keep the electrostatic integrity of devices – doping concentration into channel needs to be increased and the source and drain junctions required to become more shallower, but these trends are offset by the increased junction leakage and higher series resistances. Fully-depleted devices, double-gate devices in particular, offer significantly better electrostatic integrity and hence, better short-channel immunity [2]. In addition to excellent channel control, the FinFET transistors also offer approximately twice the on-current compare to the planar MOSFETs because of the dual gates, even without increasing channel doping. This is beneficial for the carrier mobility and results in a low gate leakage at the same time [3]. Based on discussion planar MOSFETs can be replaced by double gate MOSFETs devices at gate lengths below 50nm in order to be able to continue forth on the shrinking path [4].

## 3. DG – MOSFET Structure

Currently standard CMOS technology can be replaced by DG MOSFETs technology to increase the integration capacity of silicon technology in the near future. A DGSOI Structure consists, basically, of a silicon slab sandwiched between two oxide layers as illustrated in Fig.1.

The salient features of the DG MOSFETs are control of short-channel effects by device geometry, as compared to bulk FETs, where the short-channel effects are controlled by doping concentration; and a thin silicon channel leading to tight coupling of the gate potential with the channel potential. These features provide potential DG MOSFET advantages are reduced 2D short channel effects leading to a shorter allowable channel length compared to bulk FET, a sharper subthreshold slope is 60 mV/dec for FinFET as compared to 80 mV/dec for bulk FET as shown in Fig.3 which allows for a larger gate overdrive for the same power supply and the same off-current and better carrier transport as the channel doping is reduced [6].

Basically there are 2 kinds of DG-FETs: (1) Symmetric: - In Symmetric DG-FETs have identical gate electrode materials for the front and back gates means gate electrode material is same for both gate. When symmetrically driven, the channel is formed at both the surfaces. (2) Asymmetric: - In an asymmetric DG-FET, the top and bottom gate electrode materials can different. Channel is formed only in one surface [4].

In the fig.2 it is shown that there are three ways to fabricate the DG-FET. Types 1 and 2 suffer most from fabrication problems, viz. it is hard to fabricate both gates of the same size and that too exactly aligned to each other. Also, it is hard to align the source/drain regions exactly to the gate edges. Further, in Type 1 DG-FETs, it is hard to provide a low-resistance, area-efficient contact the bottom gate, since it is buried. The FinFET is the easiest one to fabricate as shown in fig. 4.

## 4. FinFET Structure Analysis

In Fig.2 it is shown that type 3 is called as a FinFET. This is called as FinFET because the silicon resembles the dorsal fin of a fish. It is referred to as a quasi-planar device. In the FinFET the silicon body has been rotated on its edge into a vertical orientation so only source and drain regions are placed horizontally about the body, as in a conventional planar FET. The separate biasing in DG device easily provides multiple threshold voltages [8].

A gate can also be fabricated at the top of the fin, in which case it is a triple gate FET. The width of a FinFET is quantized due to the vertical gate structure. The fin height determines the minimum transistor width (*Wmin*). With the two gates of a single-fin FET tied together, $W_{min}$ is

$$W_{min} = 2 \times H_{fin} + T_{fin} \quad (1)$$

Where $H_{fin}$ is the height of the fin and $T_{fin}$ is the thickness of the silicon body as shown in Fig. 1. $H_{fin}$ is the dominant component of the transistor width since $T_{fin}$ is typically much smaller than $H_{fin}$ Since $H_{fin}$ is fixed in a FinFET technology, multiple parallel fins are utilized to increase the width of a FinFET as shown in fig.5. The total physical transistor width ($W_{total}$) of a tied-gate FinFET with *n* parallel fins is:

$$W_{total} = n \times W_{min} = n \times (2 \times H_{fin} + T_{fin}). \quad (2)$$

FinFETs are designed to use multiple fins to achieve larger channel widths. Source/Drain pads connect the fins in parallel. As the number of fins is increased, the current through the device increases [9].
Main features of FinFET are (1) Ultra thin Si fin for suppression of short channel effects (2) Raised source/drain to reduce parasitic resistance and improve current drive (3) Gate last process with low $V_T$, high k gate

dielectrics (4) Symmetric gates yield great performance, but can built asymmetric gates that target $V_T$ [7].

The two vertical gates of a FinFET can be separated by depositing oxide on top of the silicon fin, thereby forming an independent-gate FinFET as shown in Fig. 5(b).

An independent-gate FinFET (IG-FinFET) provides two different active modes of operation with significantly different current characteristics determined by the bias conditions. Alternatively, in the Single-Gate-Mode, one gate is biased with the input signal while the other gate is disabled (disabled gate: biased with $V_{GND}$ in an N-type FinFET and with $V_{DD}$ in a P-type FinFET). The two gates are strongly coupled in the Dual of the two independent gates as shown in Fig. 7. In the Dual-Gate-Mode, the two gates are biased with the same signal -Gate-Mode, thereby lowering the threshold voltage $V_{th}$ as compared to the Single-Gate-Mode. The maximum drain current produced in the Dual-Gate-Mode is therefore 2.6 times higher as compared to the Single-Gate-Mode as shown in Fig. 7. The switched gate capacitance of the FinFET is also halved in the Single-Gate-Mode due to the disabled back gate [9].
The drain current normalized by the channel width W at the same $V_{gs}$ is almost independent of $H_{fin}$ while fixing $T_{fin}$. The small differences in the normalized drain current for devices with the same $H_{fin}$ and different $T_{fin}$ come from the threshold voltage roll-off due to the increase in $T_{fin}$ [10]. The dependences of $V_{th}$ roll-off and subthreshold swing S on $H_{fin}$ and $T_{fin}$ are shown in Figs. 8 and 9.

## 5. Fabrication Mechanism of FinFET Technology

Fig. 10 shows the FinFET fabrication process flow. As the starting material SOI wafer is used with a 400-nm thick buried oxide layer and 50-nm thick silicon film. The measured standard deviation of the silicon film thickness is around 20 A. Although the silicon film thickness determines the channel width, the variation is acceptable for the device uniformity. The larger source of process variation is the variation in gate length. As the gate length will vary process variation also vary.

The CVD $SI_3N_4$ and $SiO_2$ stack layer is deposited on top of the silicon film to make a hard mask or cover layer. The fine Si-fin is patterned by electron beam (EB) lithography with 100 keV acceleration energy. The resist pattern is slightly ashed at 5 W and 30 sec for the reduction of the Si-fin width. Then, using top $SiO_2$ layer as a hard etching mask, the SOI layer is etched. The Si is exposed only at the sides of the Si-fin as shown in Fig. 10(1). Fig. 11 shows the fabricated Si-fin width versus the design size with the EB dose as a parameter. Fine Si-fins down to 20 nm are obtained. Using EB lithography, the S/D pads with a narrow gap in between them are delineated. The $SiO_2$ and amorphous Si layers are etched and the gap between the S/D pads is formed as shown in Fig. 10(3). While the cover layer protects the Si-fin, the amorphous Si is completely removed from the side of the Si-fin. Fig. 7 shows the simulated current density distribution in the Si-fin and pad region of FinFET. The current density contour shows that the current quickly spreads into the pads. This suggests that the parasitic resistance is reduced as shown in Fig.12.
CVD $SiO_2$ is deposited to make spacers around the S/D pads. The height of the Si fin is 50 nm, and the total S/D pads thickness is 400 nm. Making use of the difference in the heights, the $SiO_2$ spacer on the sides of the Si-fin is completely removed by sufficient over etching of $SiO_2$ while the cover layer protects the Si-fin. The Si surface is exposed on the sides of the Si-fin again as shown in Fig. 10(4). During this over etching, $SiO_2$ on the S/D pads and the buried oxide are etched.

Notice that the channel width of the devices is twice the height of the Si-fins or approximately 100 nm. By oxidizing the Si surface, gate oxide as thin as 2.5 nm is grown. Because the area of Si-fin side surface is too small, we use dummy wafers to measure the oxide thickness. During gate oxidation, the amorphous Si of the S/D pads is crystallized. Also, phosphorus diffuses from the S/D pads into the Si-fin and forms the S/D extensions under the oxide spacers. Then, boron-doped $SI_{0.4}Ge_{0.6}$ is deposited as the gate material. Because the source and drain extension is already formed and covered by thick $SiO_2$ layer, no high temperature steps are required after gate deposition. Therefore, the structure is suitable to use with new high gate dielectric and metal gates that are not compatible with each other under high temperature. After delineating the gate electrode as shown in Fig. 10(5), the probing windows are etched through the oxide. We directly probe on the poly-Si and poly-SiGe pads, with no metallization used in this experiment. The total parasitic resistance due to probing is about 3000 ohms.

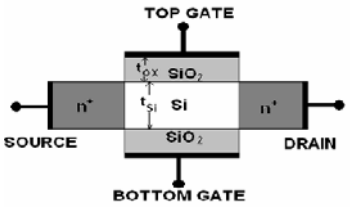
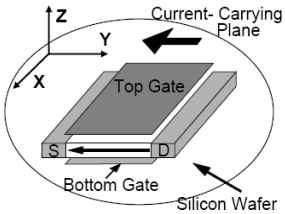
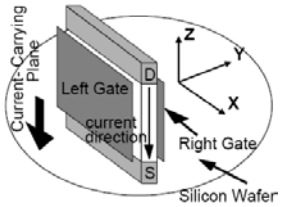


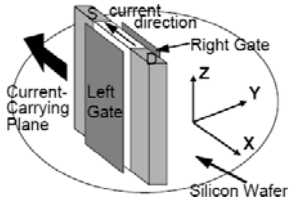

Fig. 1: Cross section of a generic planar DGFET [5]




(a) Type -1 Planar DG-FET




(b) Type-2 Vertical DG-FET




(c) Type-3 FinFET

Fig-2: Types of DG-FET (a) Planar DG-FET (b) Vertical DG-FET (c) FinFET [10]

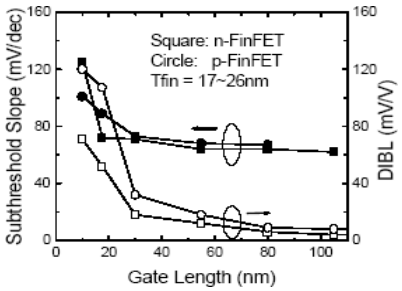



Fig.3 Short-channel effects of CMOS FinFET [3]

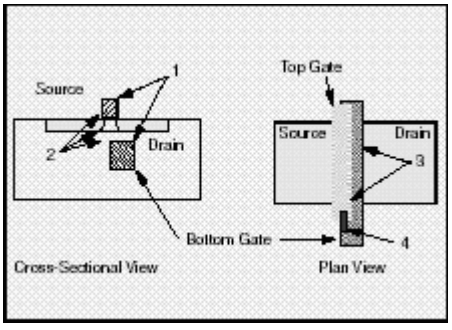
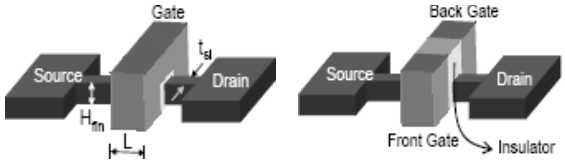
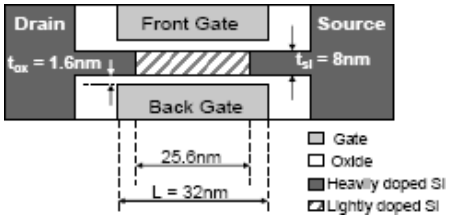



Fig.4 Schematic of the four major obstacles to DGCMOS [4]




(a) SDDG-FinFET (b) IDDG-FinFET




(c) Cross sectional top view of an independent-gate FinFET

Fig. 5 FinFET structure. (a) 3D structure of a one-fin tied-gate FinFET. (b) 3D structure of a one-fin independent-gate FinFET. (c) Cross sectional top view of an independent-gate FinFET with a drawn channel length of 32nm [9].

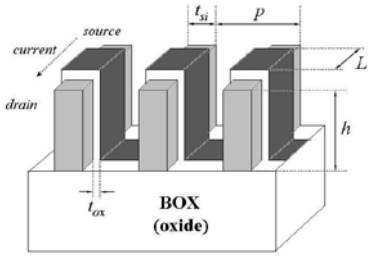



Fig.6. Multi-fin FinFET structure

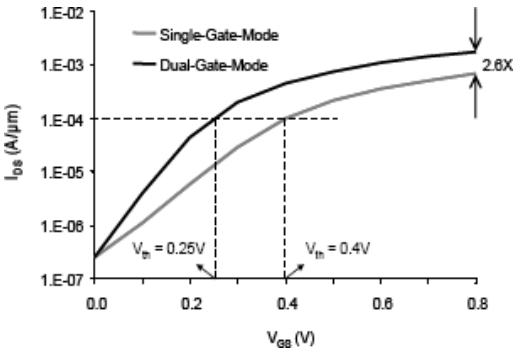



Fig. 7 Drain current characteristics of an N-type IG-FinFET. The drain-to source voltage is 0.8V. T = 70'C [9]

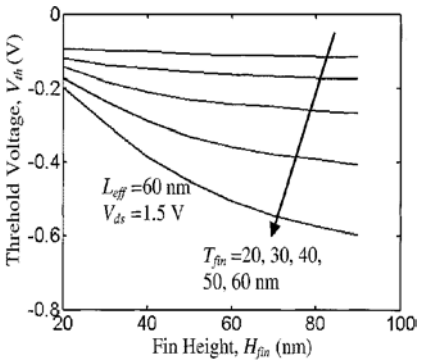



Fig. 8 Dependence of threshold voltage roll-off on $H_{fin}$ and $T_{fin}$ [10]

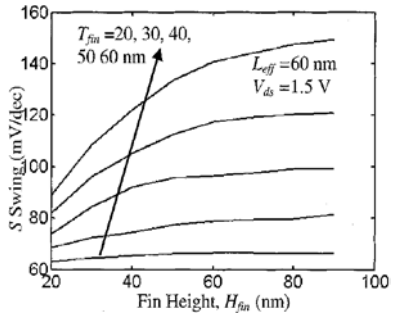



Fig. 9 Dependence of subthreshold swing on $H_{fin}$ and $T_{fin}$ [10]

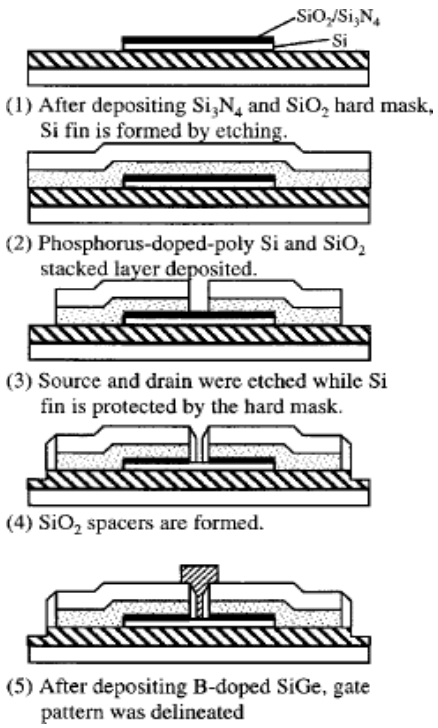



Fig.10 FinFET fabrication process flow.

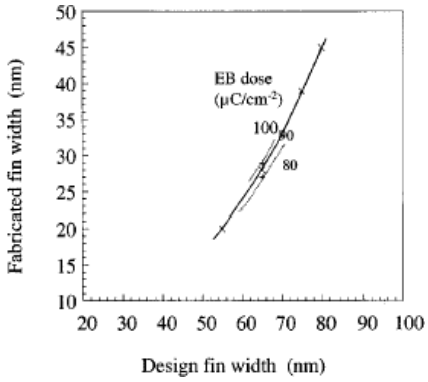



Fig. 11 Relationship between designs Si-fin width practical size with EB dose as a parameter.

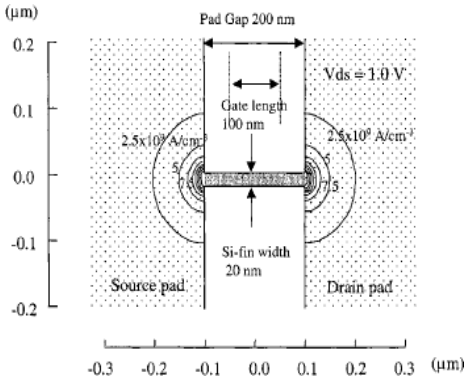



Fig. 12 Simulated current density contours in the poly-Si S/D pads. The fast spread of the current indicates effective reduction of the series resistance

## 6. Conclusions

To summarize, in FinFET due to dual gate structure it has better controlling over several short channel effect such as $V_T$ rolloff, DIBL, subthreshold swing, gate direct tunneling leakage and hot carrier effects compare to the planner MOSFET FinFET has higher integration density compare to the planner MOSFET. Also fabrication of the FinFET is easiest compare to the other two type of DG MOSFET. So particularly in nanometer regime the FinFET gives better performance compare to the planner MOSFET.

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