DESIGN COMPARISON OF DIFFERENT TECHNIQUES USED TO ESTSBLISH LOW POWER ARITHMETIC AND LOGIC UNIT

Anumol George[1], Raji Elsa Varghese[2]

[1] *PG Scholar Musaliar College of Engineering and Technology, Pathanamthitta, Kerala, India*
anugeorge2296@gmail.com

[2] *Assistant Professor Musaliar College of Engineering and Technology, Pathanamthitta, Kerala, India*
İtseisa4u@gmail.com

Abstract

An Arithmetic Logic Unit (ALU) is employed in arithmetic, logical operate altogether processor. It is also an important subsystem in digital system design. ALU is one of the most important components of any system and is used in many appliances like calculators, cell phones, and computers. We can design an arithmetic and logic unit using the arithmetic unit, a logic unit, and a multiplexer. The number of operations depends on the number of bits of an arithmetic and logic unit. Using conventional gates like AND gates & OR gates the digital system is implemented which dissipates a major amount of energy in the form of bits which gets erased during logical operation. There are different methods available to make the arithmetic and logic more efficient. Reversible logic gates, Vedic multiplier, feedback switch logic (FSL), etc. are the methods to reduce the power of an ALU. In this paper, we are focusing to discuss these methods. The slight changes in the designs are described here.

Keywords: Arithmetic and logic unit, low delay, low power, Reversible logic gates.

1 Introduction

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A register is a small amount of storage available as part of a CPU. The control unit tells the ALU what operation

to perform on that data, and the ALU stores the result in an output register. The control unit moves the data between these registers, the ALU, and memory.

An ALU performs basic arithmetic and logic operations. Examples of arithmetic operations are addition, subtraction, multiplication, and division. Examples of logic operations are comparisons of values such as NOT, AND, and OR gates.The growth of computing machines has reached great success in the past decade. Conventional technologies such as MOS transistor would reach heights because of exponential growth in transistor density and especially increasing power dissipation. Various alternatives are required to increase the computational power of the current generation.Now a day's all CPU units, any machinery parts utilize basic arithmetic operations like addition, subtraction, and multiplications. ALU plays a vital role in CPU's, Microprocessors, and Microcontrollers so ALU is the heart of the processor. The central processing unit speed greatly depends upon the ALU so we need to have fast and efficient ALU. There are different methods to achieve low power ALU.

2 Theory of Operation

As we know that ALU design is most important. They are playing a vital role in the operations of microcontrollers and microprocessors. ALU performs arithmetic and logical operations. It contains an arithmetic unit and logic unit. To select the operations we can use multiplexers. There are 8, 16, 32 bit etc. ALU‘s are available it depends upon how many arithmetic and logical operations are to be performed. For eg: we can analyze an 8-bit ALU.

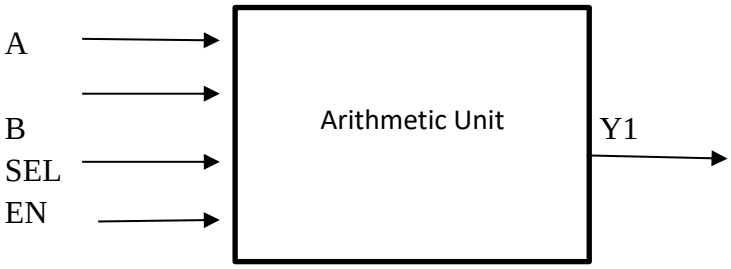

Fig. 1. Blockdiagram of Arithmetic unit

The above figure shows an arithmetic unit for an 8-bit ALU. It performs four arithmetic operations. We can select the operations to be performed. We get an 8-bit output for these operations. A and B are 8-bit inputs that are directly applied to the input of the arithmetic unit. The nature of output is based on SEL and EN signals. When the SEL line is selected corresponding operations to be performed.

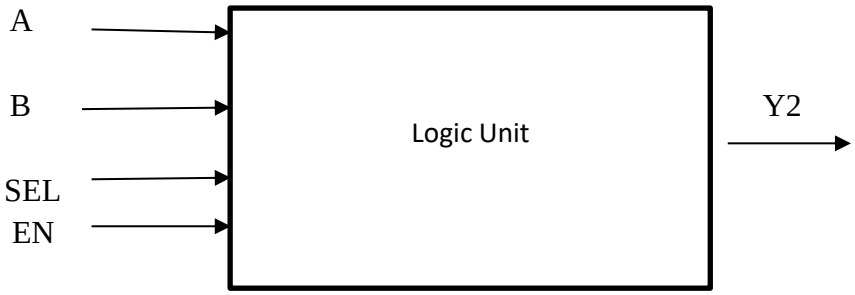

Fig. 2. Blockdiagram of Logic Unit

The above figure shows an 8-bit logic unit. It can perform 4 logical operations. The operations to be performed can be determined by us. The nature of the output is based on the SEL and EN lines.

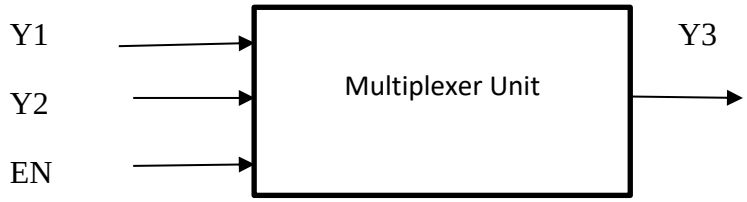

Fig. 3. Blockdiagram of Multiplexer

The given figure shows a multiplexer diagram. The outputs of both arithmetic and logic units are fed into the inputs of the MUX unit. The EN signal is used to enable the operation.The below figure shows an 8- bit ALU block diagram. The outputs of both arithmetic and logic unit are directly connected to the inputs of a multiplexer unit. It can perform 8 operations four arithmetic and four logical operations. The EN signal determines whether the arithmetic or logical operations to be performed. Depending on this corresponding operations are performed.

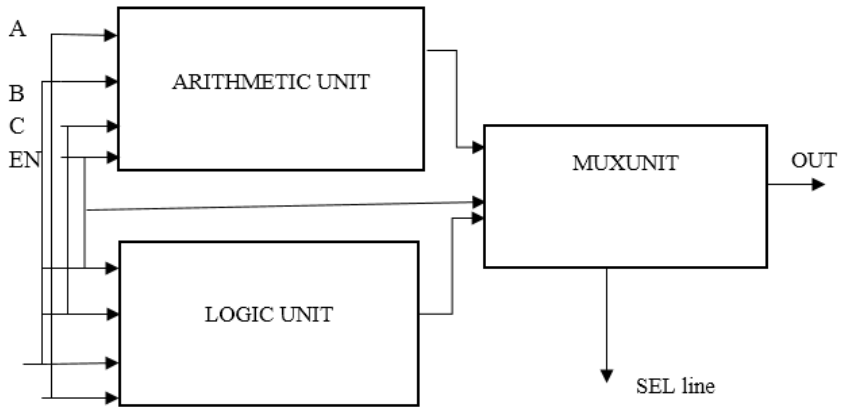

Fig. 4. Blockdiagram of Arithmetic and Logic Unit

3 Analysis of Different Design Methods

There are different methods available to make an ALU low power. The delay, power and area are analyzed in these methods. Conventional ALU is made up of AND & OR gates, but it consumes more power, area and causes delay problems. So we approached different methods to make a low power ALU. These different methods are analyzed in this section and evaluated coorectly with explanations and diagrams.

2.3 Reversible Logic Condition Using Reversible Logic Gates

Using standard gates like AND& OR gates the digital system is enforced that dissipates a serious quantity of energy within the style of bits that gets erased throughout operation by victimization reversible logic circuits in situ of standard logic, circuits the matter of energy loss are often resolved in digital circuit coming up with the changeability has become the foremost promising technology.

In today's world ALU is one of the very important of any system having many applications in computers, cell phones, calculators, etc. The design of one bit reversible ALU using a reversible logic gate is analyzed in this section. The proposed ALU is analyzed on the FPGA SPARTAN6 device. The projected style is compared in terms of propagation delay, quantum price, and garbage outputs. The 4-bit reversible ALU is also designed on proposed 1- bit reversible ALU architecture.

The arithmetic and logic unit is used to perform various arithmetic and logical operations. It is commonly used in many digital system such as mobile phones, laptops, calculators etc.

Design verification is an important step digital circuit design. There are different types design verification techniques such as functional verification and equivalence checking. In this study paper it deals with three 2x2 reversible logic gates. Here we are discussing about Feynman gate, reversible XOR gate, BME gate, R gate and DKG gates.

The arithmetic unit consists of adders, subtractors, multipliers etc. in this section we are focusing on the adders used. Parallel adder is used in ALU circuits. It is made up of full adders and 1 bit and 4 bit reversible ALU's. DKG gates are used as full adder. The input carry Cin enters the full adder at its least important bit position. Then output is taken from the full adder. The input carry Cin is initially set to 0. If Cin is 1 then add this one to the sum produced by the fulladder. They uses opcodes for arithmetic and logical operations.

By using these concept we get a highly efficient reversible ALU's. First of all it produces less delay than the existing 1 bit ALU architecture. Second this ALU can produce more arithmetic and logic operations.

Table 1. Comparsion of parameters

parameter	Proposed 4 bit ALU	Proposed 1 bit ALU	Existing 1 bit ALU
Delay	7.885 ns	6.334 ns	16 ns
Quantum Cost	88	22	24

The new design is advantageous in the case of delay and quantum cost. It has less delay than the existing 1 bit ALU. Using these we can implement n bit ALU. They are also garbage free. Here we studied about the functions of reversible logic gates and implementations of ALU using these gates. The design is successfully completed by using these gates.

3.2 Feedback Switch Logic

Low power and high-speed requirement is a challenging task in the design of ALUs. Supply voltage scaling may be a promising approach as a result of it reduces shift activities and active power however it degrades the performance and hardiness. Recently a replacement dynamic like static circuit family known as Feedback-Switch Logic (FSL) has been projected. FSL is appropriate for prime speed and low power as a result of it offers quick shift, reduced capacitance and input-switching dependent activity factor without the need for clock connection.

FSL combines high-performance domino with the activity-dependent low power consumption of static circuits. Also, FSL has advantages of reduced capacitance and fast switching speed. It has a 14% reduction in delay comparable to static logic circuits and power consumption is comparable to static CMOS logic circuits.

The major research problem is to design a high speed and low power circuit using CMOS technology. There are different logic families are available and they can achieve high speed than the conventional CMOS technology. FSL is the best design among the logic families. To improve the performance of the microprocessor we have to reduce the power consumption, then we can design a high speed and low power microprocessors. We have to reduce the power consumption of all the components in the circuit. The major component which produces the large power consumption is the ALU. So we are focusing to reduce the power of the ALU unit.

The FSL is a clock less differential circuit and it produces the output and its complement in the single side of the gate. In the design of an ALU it consists of four parts such as arithmetic unit, control unit, logic unit and shifter circuit. Then we have to focus these units individually

and analyze their power and delay. Then we compare the power and delay occurred by the conventional CMOS circuits and the FSL .

Table 2. Comparison of power and delay of logical operation

Logical operation	Power consumption		Delay	
	CMOS	FSL	CMOS	FSL
AND	434.3	461.2	340.7	284.4
OR	471.9	495.9	397.6	339.3
XOR	504.8	539.3	403	357.1

2.5 Low Power Vedic Multiplier

Multipliers are implemented in the digital system using the multiple numbers of adders and such multipliers are implemented with the help of array and booth algorithms. But Vedic mathematics illustrates the multiplication operation very faster than other algorithms by reducing the number of addition. The reduced number of adders in Vedic multiplier minimizes the operating delay and area of device with less number of adders. The low power and area efficient logic block reversible logic based adder and Vedic multipliers are integrated to construct architecture of ALU resulted that the power dissipation of the proposed ALU unit is reduced in comparison with the standard unit. The use of fewer adders in the Vedic multiplier reduces the area and power dissipation of the ALU system.

The reversible logic circuits provides a new direction for low power circuits. This reversible logic gates has less power consumption and delay compared to the conventional circuits. An arithmetic unit contains adders, substractors and multipliers. In this section we are discussing about the implementation of an 8-bit Vedic multiplier rather than conventional multipliers such as array multiplier, Braun multiplier, modified booth multiplier and Wallace tree multiplier. And also verified that its propagation delay is less compared the conventional system.

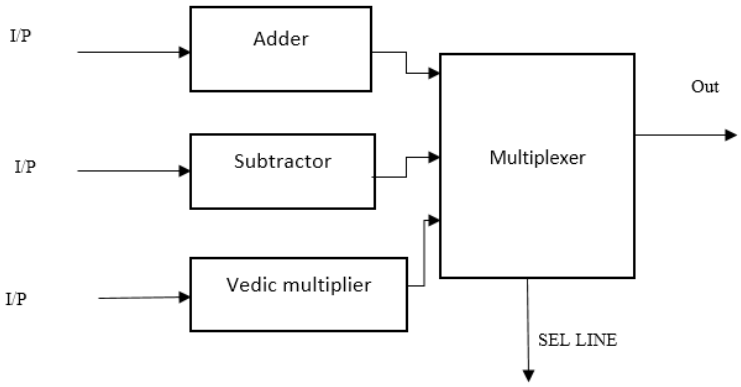

Fig. 5. Proposed Arithmetic and Logic Unit

The block diagram shows that ALU unit consists of arithmetic unit, logic unit and a multiplexer. The arithmetic unit performs addition, subtraction, multiplication and division. The logic unit performs logical operations such as AND, OR, NOT etc., using basic logic gates with reversible logic.

Commonly multipliers are employed with multiple number of adders and these are implemented with the help of array and booth algorithms. By using Vedic multipliers we can perform fast multiplication operation than any other algorithms. So it minimizes the number of adders therefore the operating delay and area of the device are minimized. Reversible logic based adders and a Vedic multiplier is integrated to construct a low power and high performance ALU. As a result the power dissipation is reduced. By using less number of adders in a Vedic multiplier helps to reduce the power and area. The proposed technique consumes the 35% of power, area of 23% less and the 17% of higher performance compared to conventional ALU circuit.

3.3 Design of 16 Bit ALU Using Reversible Logic Gates

Energy loss is important in the modern VLSI system. Conventional ALU uses AND & OR gates, it has high power dissipation and delay. We have to design a low power ALU. We came to reversible logic gates. One of the methods using a reversible logic gate is explained above.

Here we are using another reversible logic gates. The design of a 16-bit arithmetic and logic unit consists of 8 arithmetic and 8 logical operations. A reversible logic gates consist of the same number of inputs and outputs, e.g.: for an n – input n- output will be produced. The ALU unit can be designed by using various methods such as reversible logic gates, irreversible, pass transistor, etc. here we are focusing on two types which are reversible ALU using all reversible logic gates and reversible ALU using Toffoli gate.In this paper, the multifunction ALU based on reversible logic gates has been designed which contains the

reversible control unit and the reversible full adder. The reversible control unit and the reversible full adder are cascaded and arbitrary bit reversible ALU modules can be realized in this way. Here 1bit ALU has been designed. The A and B inputs of the reversible management unit ar altered looking on the S0, S1and S2 values and applied as input to reversible full adder using D Peres gates. By controlling one of the inputs to the adder, various arithmetic and logic operations can be realized. The designed circuit has 3 management signals with a provision for realizing eight arithmetic operations and 4 logic operations.

The reversible ALU can implement by using a 3*3 Toffoli logic gate The multi-function ALU based on reversible Toffoli logic gates mainly contains the reversible function generator (FUNC) and the reversible controlled unit (DXOR). The reversible perform generator and therefore the reversible controlled unit ar cascaded by some n-Toffoli gates and NOT gates, and discretional bit reversible ALU modules may be complete during this means. In the procedure of cascading the reversible function generator and the reversible controlled unit, we reuse the output signals to reduce the cost of circuit design as much as possible.

4 Conclusion

Different ALU designs are discussed. Conventional ALU design is Based on the AND & OR gates. Its power consumption and delay are high. So to reduce these effects we discussed some of the methods.

In the case of reversible logic, we use reversible logic gates in the place of basic logic gates. It effectively reduces the area, delay and power consumption than conventional. In the case of feedback switch logic static CMOS is replaced by FSL. FSL is appropriate for prime speed and low power as a result of it offers quick switch, reduced capacitance. Then in the case of low power Vedic multiplier. We are replacing conventional multipliers with Vedic multiplier. It can reduce number of adders used in the circuit thereby reducing the power dissipation and delay.

References

1. *Esther Rani, T., Asha Rani, M., Rameshwar Rao.: Area optimized low power arithmetic and logic unit, 2013 3rd int conference on electronics computer technology, 07 .ISBN 978-1-4244-8679-3, 978-1-4244-8678-6 (2011)*

2. *Senthil Sivakumar, M., Sundaram, A., Gurumekala, T., Banupriya, M.: Design of ALU using reversible logic based Low Power Vedic Multiplier, International Journal of Scientific & Engineering Research, Volume 6, Issue 2, February(2015)*
3. *Arindam Banerjee and Debesh Kumar Das.: A New ALU Architecture Design using Reversible Logic, 2016 Sixth International Symposium on Embedded Computing and System Design (ISED) 978-1-5090- 2541-1/16 IEEE(2016)*
4. *Patanjali Prakash and Sarema, A.K.: Design of Low Power High Speed ALU Using Feedback Switch Logic, 2009 International Conference on Advances in Recent Technologies in Communication and Computing 978-0-7695-3845-7/09 IEEE(2009)*
5. *Shalem, R., John, E., John, L.K.: A novel low-power energy recovery full adder cell* Proc. Great Lakes Symp. VLSI, *pp. 380-383(1999)*
6. *Chandrakasan, P., Sheng, S., Broderson, R.W.: Low-power CMOS digital design",* IEEE J. Solid-State Circuits, *vol. 27, pp. 473-483, Apr. (1992)*
7. *Shoba, M., Nakkeeran.: GDI based full adders for energy efficient arithmetic applications, Engineering Science and Technology, an International Journal, vol. 19, no. 1, pp. 485–496, Mar. (2016)*
8. *Ramkumar, B., Kittur, H.M.: Low-power and area efficient carry-select adder,* IEEE Trans. Very Large Scale Integr. (VLSI) Syst., *vol. 20, no. 2, pp. 371-375, Feb. (2012)*